DISCRETE SEMICONDUCTORS

Discrete Semiconductor Packages

Data Handbook SC18
1999

PHILIPS

Let's make things better.

http://www.semiconductors.philips.com

QUALITY ASSURED

Our quality system focuses on the continuing high quality of our components and the best possible service for our customers. We have a three-sided quality strategy: we apply a system of total quality control and assurance; we operate customer-oriented dynamic improvement programmes; and we promote a partnering relationship with our customers and suppliers.

PRODUCT SAFETY

In striving for state-of-the-art perfection, we continuously improve components and processes with respect to environmental demands. Our components offer no hazard to the environment in normal use when operated or stored within the limits specified in the data sheet.

Some components unavoidably contain substances that, if exposed by accident or misuse, are potentially hazardous to health. Users of these components are informed of the danger by warning notices in the data sheets supporting the components. Where necessary the warning notices also indicate safety precautions to be taken and disposal instructions to be followed. Obviously users of these components, in general the set-making industry, assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be ‘chemical’, ‘special’ or sometimes ‘industrial’ waste. Disposal as domestic waste is usually not permitted.

Preface

TABLE OF CONTENTS

Preface

Preface

INTRODUCTION

Philips Semiconductors is one of the world's leading suppliers of discretes. Our range stretches from small-signal diodes and transistors, through FET power-devices and power rectifiers and triacs, to RF and microwave devices and modules. Such a diverse range of devices requires an equally diverse range of package designs. These packages must not only protect the enclosed circuit and connect it to the outside world, but must also ensure the device operates at its optimum performance in a wide variety of applications.

The discrete semiconductor package, which for many years was only an afterthought in the design and manufacture of electronic systems, increasingly is being recognized as a critical factor in both cost and performance. Indeed, in many applications, the package is often as important as the circuit it encapsulates. And as the functional density of devices and systems increases, the role of the discrete semiconductor package and its interconnections becomes ever more important.

With this in mind, this publication consolidates all relevant data for Philips Semiconductors discrete packages in one book – from dimensional outline drawings and soldering information, to thermal design considerations, packing data, and chemical content tables. It should be viewed as a logical extension to our Discrete Semiconductor Data Handbook series and, as such, is intended to serve as a practical data reference to all those involved in production and engineering design, as well as a guide to package selection and availability.

An innovative partner

The development of discrete semiconductor packages is a dynamic technology as new and improved circuit processes become available. Applications that until only a few years ago were unattainable, are today common place. From mobile telecommunications and satellite broadcasting to aerospace and automotive applications, each imposes its own individual demands on the electronic package.

To meet these, and future demands, it is essential that the component manufacturer has an intimate knowledge of the multidisciplinary technologies involved to bring the circuit and package together in an optimum design.

Here at Philips, we have been involved in discrete semiconductor package design and development since the early1950's, during which time we have built up a wealth of experience and know-how in advanced process technologies and assembly procedures. By fully exploiting this expertise, and establishing close working partnerships with our customers, we have developed many market-driven and innovative package designs.

How this book is organized

We organized this databook into the following chapters:

Chapter 1 gives an overview of our discrete semiconductor packages along with a 3-dimensional illustration of each type. Packages are listed in ascending order of Philips outline code and followed by cross-reference lists from the JEDEC and EIAJ numbers to the equivalent Philips SOD/SOT number, where applicable.

Chapter 2 contains outline dimensional drawings for most of our discrete packages.

Chapter 3 reviews discrete package handling precautions with emphasis on ESD awareness at the assembly workstation.

Chapter 4 covers through-hole and SMD soldering and mounting techniques, and includes recommended footprint designs for many SMD packages.

Chapter 5 is divided into three parts covering: essential thermal properties of discrete semiconductors, worked examples of junction temperatures, and component heat dissipation and heatsink design.

Chapter 6 contains a survey of some of the packing methods most frequently used and includes the dimensions and shapes of the packing boxes and reels as well as their packing quantities.

Chapter 7 provides comprehensive data on the chemical composition of our discrete devices with information on their disposal and safety.

For information about IC packages, refer to Philips Semiconductors' Data Handbook IC26 *Integrated Circuit Packages,* order number 9398 652 90011.

Preface

CHAPTER 1

PACKAGE OVERVIEW

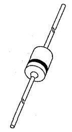
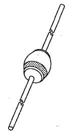
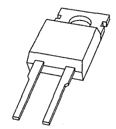
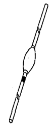
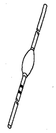
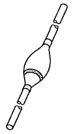
Package overview

Chapter 1

PACKAGE OVERVIEW

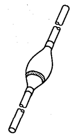
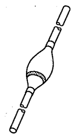
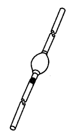
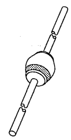
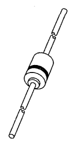
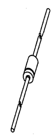
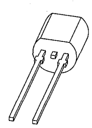
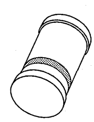
The following table contains a listing of discrete packages in ascending order. The list contains the description of the various packages with their 3-dimensional view and the page number on which the outline drawing can be found. Cross-references from the JEDEC and EIAJ numbers to the equivalent SOD/SOT numbers, where applicable, can be found after this table.

PACKAGES IN ASCENDING ORDER OF SOD/SOT NUMBERS

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOD27	Hermetically sealed glass package; axial leaded; 2 leads		2 - 2
SOD57	Hermetically sealed glass package; axial leaded; 2 leads		2 - 2
SOD59	Plastic single-ended package; heatsink mounted; 1 mounting hole; 2-lead TO-220		2 - 3
SOD61A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 4
SOD61AB to AK	Hermetically sealed glass package; axial leaded; 2 leads		2 - 5
SOD61AB2	Hermetically sealed glass package; axial leaded; 2 leads		2 - 6

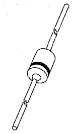
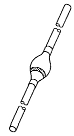
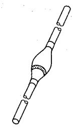
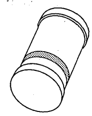
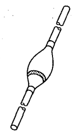
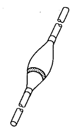
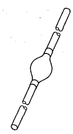
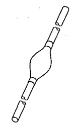
Package overview

Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOD61AC2	Hermetically sealed glass package; axial leaded; 2 leads		2 - 6
SOD61AD2	Hermetically sealed glass package; axial leaded; 2 leads		2 - 7
SOD61H2	Miniature hermetically sealed glass package; axial leaded; 2 leads		2 - 7
SOD64	Hermetically sealed glass package; axial leaded; 2 leads		2 - 8
SOD66	Hermetically sealed glass package; axial leaded; 2 leads		2 - 8
SOD68	Hermetically sealed glass package; axial leaded; 2 leads		2 - 9
SOD70	Plastic near cylindrical single-ended package; 2 in-line leads		2 - 10
SOD80C	Hermetically sealed glass surface mounted package; 2 connectors		2 - 11

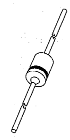
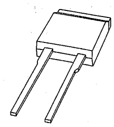
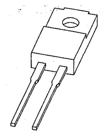
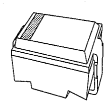
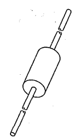
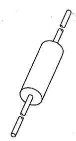
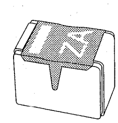
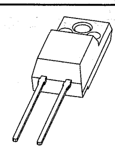
Package overview

Chapter 1

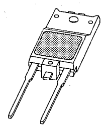
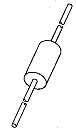
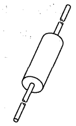
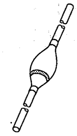
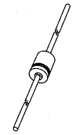
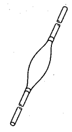
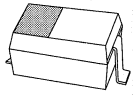
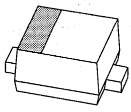
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOD81	Hermetically sealed glass package; Implotec$^{TM(1)}$ technology; axial leaded; 2 leads		2 - 11
SOD83A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 12
SOD83B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 12
SOD87	Hermetically sealed glass surface mounted package; Implotec$^{TM(1)}$ technology; 2 connectors		2 - 13
SOD88A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 13
SOD88B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 14
SOD89A	Hermetically sealed glass package; axial leaded; 2 leads		2 - 14
SOD89B	Hermetically sealed glass package; axial leaded; 2 leads		2 - 15

Package overview

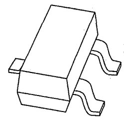
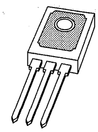
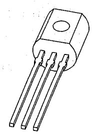
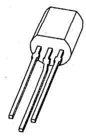
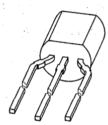
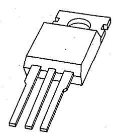
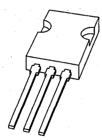
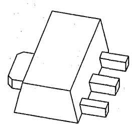
Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOD91	Hermetically sealed glass package; Implotec™(1) technology; axial leaded; 2 leads		2 - 15
SOD95	Plastic single-ended package; 2-lead low-profile TO-220		2 - 16
SOD100	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-lead TO-220F exposed tabs		2 - 17
SOD106	Transfer-moulded thermo-setting plastic small rectangular surface mounted package; 2 connectors		2 - 18
SOD107A	Hermetically sealed plastic package; axial leaded; 2 leads		2 - 19
SOD107B	Hermetically sealed plastic package; axial leaded; 2 leads		2 - 19
SOD110	Very small ceramic rectangular surface mounted package		2 - 20
SOD113	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-lead TO-220 'full pack'		2 - 21

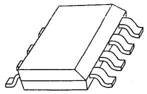
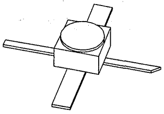
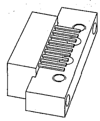
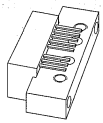
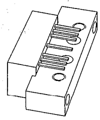
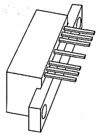
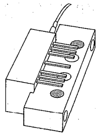
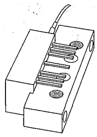
Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOD117	Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads (one lead cropped)		2 - 22
SOD118A	Hermetically sealed plastic package; axial leaded; 2 leads		2 - 23
SOD118B	Hermetically sealed plastic package; axial leaded; 2 leads		2 - 23
SOD119AB	Hermetically sealed glass package; axial leaded; 2 leads		2 - 24
SOD120	Hermetically sealed glass package; axial leaded; 2 leads		2 - 24
SOD121AB to AJ	Hermetically sealed glass package; axial leaded; 2 leads		2 - 25
SOD323	Plastic surface mounted package; 2 leads		2 - 26
SOD523	Plastic surface mounted package; 2 leads		2 - 27

Package overview Chapter 1

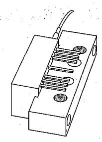
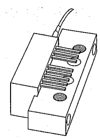
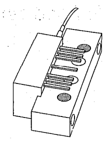
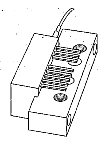
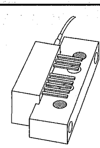
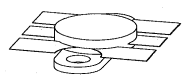
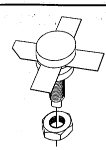
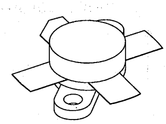
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT23	Plastic surface mounted package; 3 leads		2 - 28
SOT32	Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads		2 - 29
SOT54	Plastic single-ended leaded (through hole) package; 3 leads		2 - 30
SOT54 variant	Plastic single-ended leaded (through hole) package; 3 leads (on-circle)		2 - 31
SOT54A	Plastic single-ended leaded (through hole) package; 3 leads (wide pitch)		2 - 32
SOT78	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB		2 - 33
SOT82	Plastic single-ended package; 3 leads (in-line)		2 - 34
SOT89	Plastic surface mounted package; collector pad for good heat transfer; 3 leads		2 - 35

Package overview Chapter 1

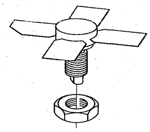
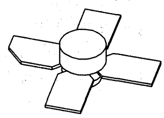
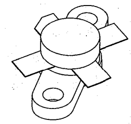
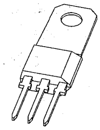
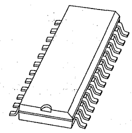
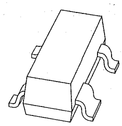
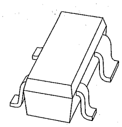
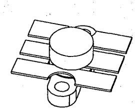
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT96-1 (SO8)	Plastic small outline package; 8 leads; body width 3.9 mm		2 - 36
SOT100A	Surface mounted ceramic hermetic package; 4 leads		2 - 37
SOT115D	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 9 gold-plated in-line leads		2 - 38
SOT115G	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads		2 - 39
SOT115J	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 7 gold-plated in-line leads		2 - 40
SOT115L	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 7 gold-plated in-line leads		2 - 41
SOT115N	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 42
SOT115P	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 43

Package overview

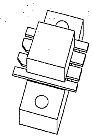
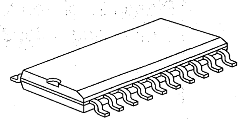
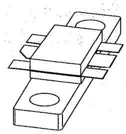
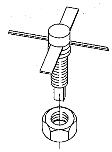
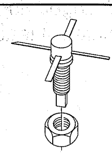
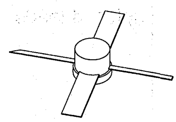
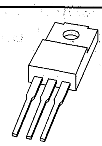
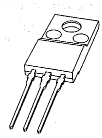
Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT115R	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 44
SOT115T	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 8 gold-plated in-line leads		2 - 45
SOT115U	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 7 gold-plated in-line leads		2 - 46
SOT115V	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads		2 - 47
SOT115W	Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 8 gold-plated in-line leads		2 - 48
SOT119A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 49
SOT120A	Studded ceramic package; 4 leads		2 - 50
SOT121B	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 51

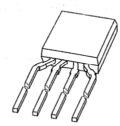
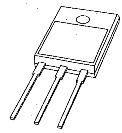
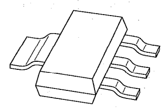
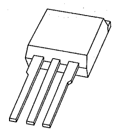
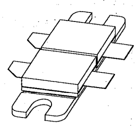
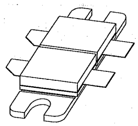
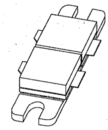
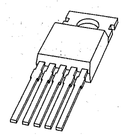
Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT122A	Studded ceramic package; 4 leads		2 - 52
SOT122D	Studless ceramic package; 4 leads		2 - 53
SOT123A	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 54
SOT128B	Plastic single-ended leaded (through hole) package; with cooling fin, mountable to heatsink, 1 mounting hole; 3 leads (in-line)		2 - 55
SOT137-1 (SO24)	Plastic small outline package; 24 leads; body width 7.5 mm		2 - 56
SOT143B	Plastic surface mounted package; 4 leads		2 - 57
SOT143R	Plastic surface mounted package; reverse pinning; 4 leads		2 - 58
SOT160A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 59

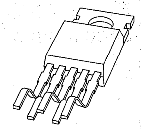
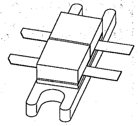
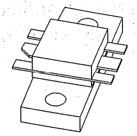
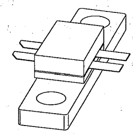
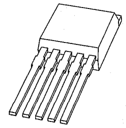
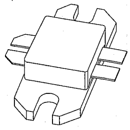
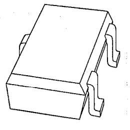
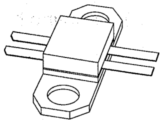
Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT161A	Flanged ceramic package; 2 mounting holes; 8 leads		2 - 60
SOT163-1 (SO20)	Plastic small outline package; 20 leads; body width 7.5 mm		2 - 61
SOT171A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 62
SOT172A1	Studded ceramic package; 4 leads		2 - 63
SOT172A2	Studded ceramic package; 4 leads		2 - 64
SOT172D	Studless ceramic package; 4 leads		2 - 65
SOT186	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 exposed tabs		2 - 66
SOT186A	Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220		2 - 67

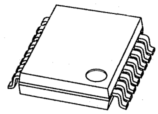
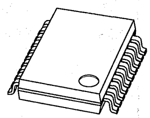
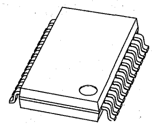
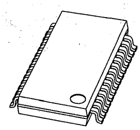
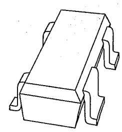
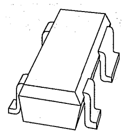
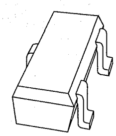
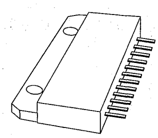
Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT195	Plastic single-ended flat package; 4 in-line leads		2 - 68
SOT199	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line)		2 - 69
SOT223	Plastic surface mounted package; collector pad for good heat transfer; 4 leads		2 - 70
SOT226	Plastic single-ended package; 3 lead low-profile TO-220		2 - 71
SOT262A1	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 72
SOT262A2	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 73
SOT262B	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 74
SOT263	Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220		2 - 75

Package overview Chapter 1

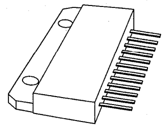
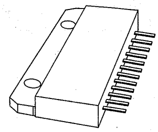
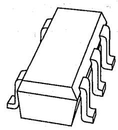
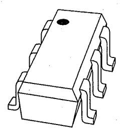
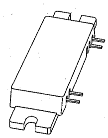
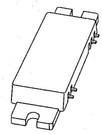
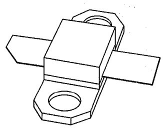
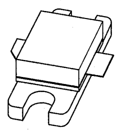
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT263-01	Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220 lead form option		2 - 76
SOT268A	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 77
SOT273A	Flanged ceramic package; 2 mounting holes; 6 leads		2 - 78
SOT279A	Flanged double-ended ceramic package; 2 mounting holes; 4 leads		2 - 79
SOT281	Plastic single-ended package; 5-lead low-profile TO-220		2 - 80
SOT289A	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 81
SOT323	Plastic surface mounted package; 3 leads		2 - 82
SOT324B	Flanged ceramic package; 2 mounting holes; 4 leads		2 - 83

Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT338-1 (SSOP16)	Plastic shrink small outline package; 16 leads; body width 5.3 mm		2 - 84
SOT339-1 (SSOP20)	Plastic shrink small outline package; 20 leads; body width 5.3 mm		2 - 85
SOT340-1 (SSOP24)	Plastic shrink small outline package; 24 leads; body width 5.3 mm		2 - 86
SOT341-1 (SSOP28)	Plastic shrink small outline package; 28 leads; body width 5.3 mm		2 - 87
SOT343N	Plastic surface mounted package; 4 leads		2 - 88
SOT343R	Plastic surface mounted package; reverse pinning; 4 leads		2 - 89
SOT346	Plastic surface mounted package; 3 leads		2 - 90
SOT347	Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads		2 - 91

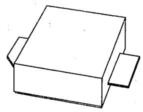
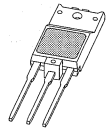
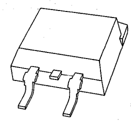
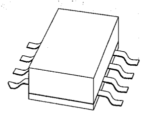
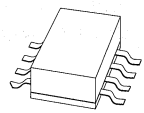
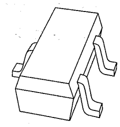
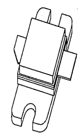
Package overview

Chapter 1

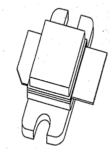
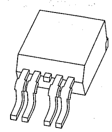
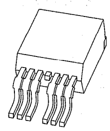
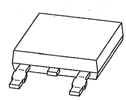
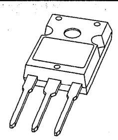
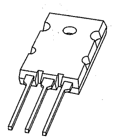
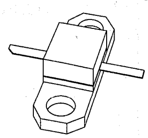
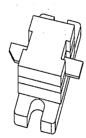
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT347B	Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads		2 - 92
SOT347C	Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads		2 - 93
SOT353	Plastic surface mounted package; 5 leads		2 - 94
SOT363	Plastic surface mounted package; 6 leads		2 - 95
SOT365A	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads		2 - 96
SOT365B	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads		2 - 97
SOT390A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 98
SOT391A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 99

Package overview

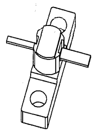
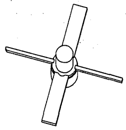
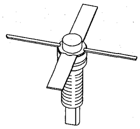
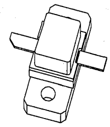
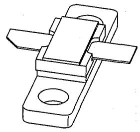
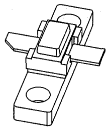
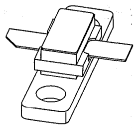
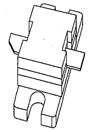
Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT391B	Flangeless ceramic package; 2 leads		2 - 100
SOT399	Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads		2 - 101
SOT404	Plastic single-ended surface mounted package (Philips version of D^2-PAK); 3 leads (one lead cropped)		2 - 102
SOT409A	Ceramic surface mounted package; 8 leads		2 - 103
SOT409B	Ceramic surface mounted package; 8 leads		2 - 104
SOT416	Plastic surface mounted package; 3 leads		2 - 105
SOT422A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 106

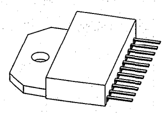
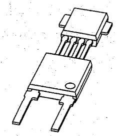
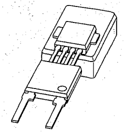
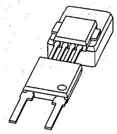
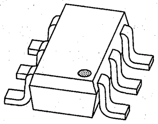
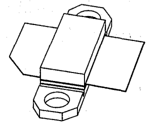
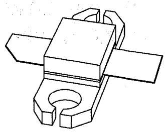
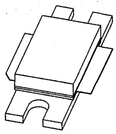
Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT423A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 107
SOT426	Plastic single-ended surface mounted package (Philips version of D^2-PAK); 5 leads (one lead cropped)		2 - 108
SOT427	Plastic single-ended package (Philips version of D^2-PAK); 7 leads (one lead cropped)		2 - 109
SOT428	Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)		2 - 110
SOT429	Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3 lead TO-247		2 - 111
SOT430	Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 lead JUMBO TO-247		2 - 112
SOT437A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 113
SOT439A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 114

Package overview Chapter 1

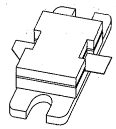
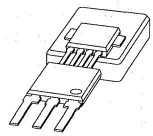
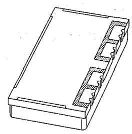
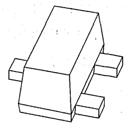
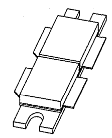
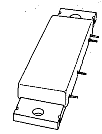
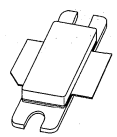
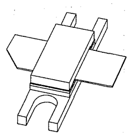
OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT440A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 115
SOT441A	Studless ceramic package; 4 leads		2 - 116
SOT442A	Studded ceramic package; 4 leads		2 - 117
SOT443A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 118
SOT445A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 119
SOT445B	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 120
SOT445C	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 121
SOT448A	Flanged hermetic ceramic package; 2 mounting holes; 2 leads		2 - 122

Package overview Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT451A	Ceramic single-ended flat package; heatsink mounted; 1 mounting hole; 11 in-line gold-metallized leads		2 - 123
SOT453A	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (3.8 x 2 x 0.8 mm); 2 in-line leads		2 - 124
SOT453B	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8 x 8 x 4.5 mm); 2 in-line leads		2 - 125
SOT453C	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 3 mm); 2 in-line leads		2 - 126
SOT457	Plastic surface mounted package; 6 leads		2 - 127
SOT460A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 128
SOT467A	Flanged LDMOST package; 2 mounting holes; 2 leads **Package under development**(2)		2 - 129
SOT468A	Flanged ceramic (AIN) package; 2 mounting holes; 2 leads		2 - 130

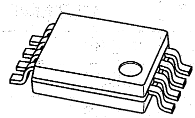
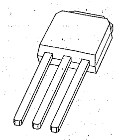
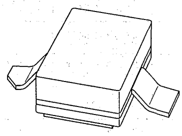
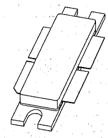
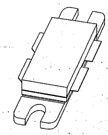
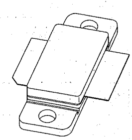
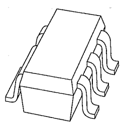
Package overview

Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT473A	Flanged ceramic package; 2 mounting holes; 2 leads **Package under development**(2)		2 - 131
SOT477B	Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8 x 8 x 4.5 mm); 3 in-line leads		2 - 132
SOT482B	Leadless surface mounted package; plastic cap; 4 terminations		2 - 133
SOT490	Plastic surface mounted package; 3 leads		2 - 134
SOT494A	Flanged double-ended ceramic (AlN) package; 2 mounting holes; 4 leads **Package under development**(2)		2 - 135
SOT501A	Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads		2 - 136
SOT502A	Flanged LDMOST package; 2 mounting holes; 2 leads **Package under development**(2)		2 - 137
SOT504A	Flanged ceramic package; 2 mounting holes; 2 leads		2 - 138

Package overview

Chapter 1

OUTLINE	DESCRIPTION	3D VIEW (not to scale)	PAGE
SOT530-1 (TSSOP8)	Plastic thin shrink small outline package; 8 leads; body width 4.4 mm		2 - 139
SOT533	Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line)		2 - 140
SOT538A	Ceramic surface mounted package; 2 leads **Package under development**(2)		2 - 141
SOT539A	Flanged balanced LDMOST package; 2 mounting holes; 4 leads **Package under development**(2)		2 - 142
SOT540A	Flanged balanced LDMOST package; 2 mounting holes; 4 leads **Package under development**(2)		2 - 143
SOT541A	Flanged LDMOST package; 2 mounting holes; 2 leads **Package under development**(2)		2 - 144
SOT551A	Plastic surface mounted package; 5 leads **Package under development**(2)		2 - 145

Notes

1. Implotec is a trademark of Philips.
2. Philips Semiconductors reserves the right to make changes without notice.

Package overview

Chapter 1

CROSS-REFERENCE FROM JEDEC TO SOD/SOT

JEDEC	OUTLINE	PAGE
DO-34	SOD68	2 - 9
DO-35	SOD27	2 - 2
DO-41	SOD66	2 - 8
DO-214AC	SOD106	2 - 18
MO-150AC	SOT338-1 / SSOP16	2 - 84
MO-150AE	SOT339-1 / SSOP20	2 - 85
MO-150AG	SOT340-1 / SSOP24	2 - 86
MO-150AH	SOT341-1 / SSOP28	2 - 87
MO-153AA	SOT530-1 / SSOP28	2 - 139
MS-012AA	SOT96-1 / SO8	2 - 36
MS-013AC	SOT163-1	2 - 61
MS-013AD	SOT137-1 / SO24	2 - 56
TO-92	SOT54	2 - 30
TO-126	SOT32	2 - 29
TO-202AA	SOT128B	2 - 55
TO-220	SOD95	2 - 16
TO-220	SOT226	2 - 71
TO-220	SOT263	2 - 75
TO-220	SOT263-01	2 - 76
TO-220	SOT281	2 - 80
TO-220AB	SOT78	2 - 33
TO-220AC	SOD59	2 - 3
TO-220F	SOD100	2 - 17
TO-220F	SOD113	2 - 21
TO-220F	SOT186	2 - 66
TO-220F	SOT186A	2 - 67
TO-236	SOT346	2 - 90
TO-236AB	SOT23	2 - 28
TO-243	SOT89	2 - 35
TO-247	SOT429	2 - 111

CROSS-REFERENCE FROM EIAJ TO SOD/SOT

EIAJ	OUTLINE	PAGE
SC-40	SOD27	2 - 2
SC-43	SOT54	2 - 30
SC-46	SOT78	2 - 33
SC-53	SOT128B	2 - 55
SC-59	SOT346	2 - 90
SC-61B	SOT143R	2 - 58
SC-62	SOT89	2 - 35
SC-63	SOT428	2 - 110
SC-67	SOT186	2 - 66
SC-70	SOT323	2 - 82
SC-73	SOT223	2 - 70
SC-74	SOT457	2 - 127
SC-75	SOT416	2 - 105
SC-76	SOD323	2 - 26
SC-79	SOD523	2 - 27
SC-88	SOT363	2 - 95
SC-88A	SOT353	2 - 94
SC-89	SOT490	2 - 134

CHAPTER 2

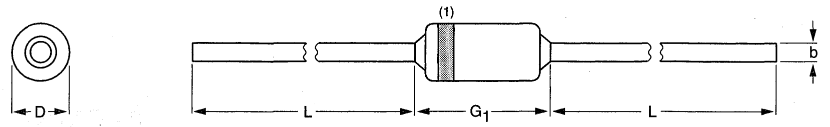
PACKAGE OUTLINES

Package outlines

Chapter 2

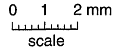
Hermetically sealed glass package; axial leaded; 2 leads

SOD27



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G_1 max.	L min.
mm	0.56	1.85	4.25	25.4



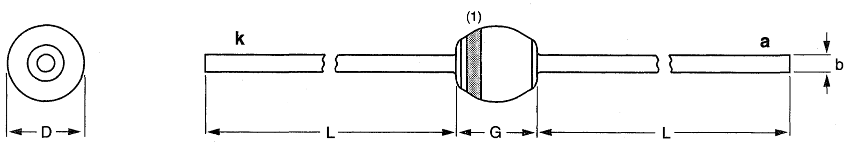
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD27	A24	DO-35	SC-40			97-06-09

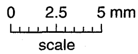
Hermetically sealed glass package; axial leaded; 2 leads

SOD57



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.81	4.57	28

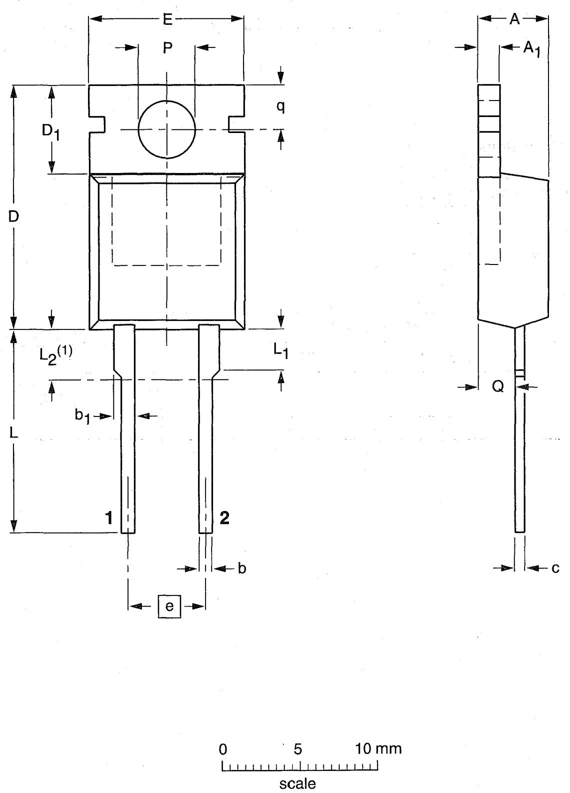


Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD57						97-10-14

Plastic single-ended package; heatsink mounted; 1 mounting hole; 2-lead TO-220 **SOD59**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	5.08	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

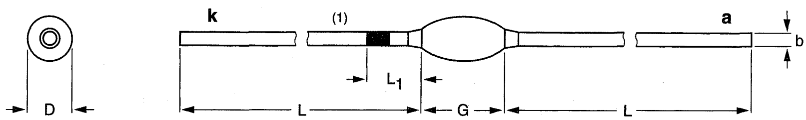
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD59		2-lead TO-220				97-06-11

Package outlines

Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads — SOD61A



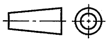
DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.	L_1 max.
mm	0.6	2.5	4.9	32.5	3

0 2.5 5 mm
scale

Note

1. The marking band indicates the cathode.

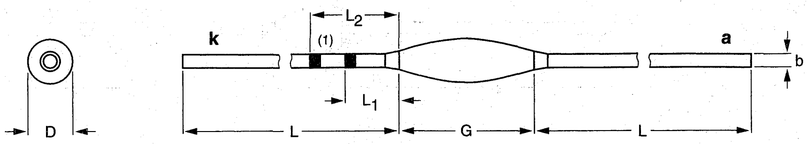
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61A						97-06-09

Package outlines

Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads

SOD61AB to AK

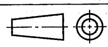


DIMENSIONS (mm are the original dimensions)

OUTLINE VERSION	UNIT	b	D max.	G max.	L min.	L_1 max.	L_2 max.
SOD61AB	mm	0.6	2.5	5.5	31.8	3	5
SOD61AC	mm	0.6	2.5	8.3	30.4	3	5
SOD61AD	mm	0.6	2.5	8.7	30.2	3	5
SOD61AE	mm	0.6	2.5	9.1	30.0	3	5
SOD61AF	mm	0.6	2.5	9.5	29.8	3	5
SOD61AG	mm	0.6	2.5	9.9	29.6	3	5
SOD61AH	mm	0.6	2.5	10.5	29.3	3	5
SOD61AI	mm	0.6	2.5	11.5	28.8	3	5
SOD61AJ	mm	0.6	2.5	12.5	28.3	3	5
SOD61AK	mm	0.6	2.5	13.5	27.8	3	n.a

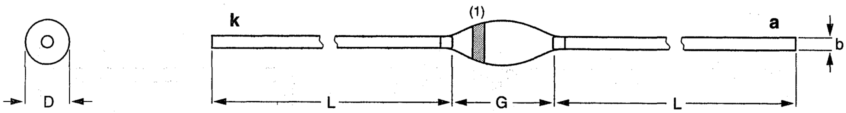
Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61AB to AK						97-06-20

Hermetically sealed glass package; axial leaded; 2 leads

SOD61AB2



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.
mm	0.6	2.5	5.5	31.8

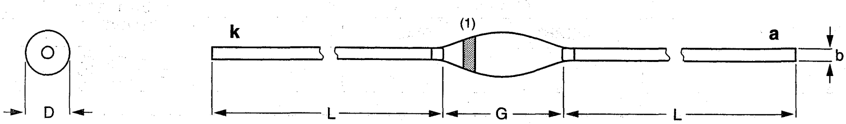
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61AB2						98-12-04

Hermetically sealed glass package; axial leaded; 2 leads

SOD61AC2



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.
mm	0.6	2.5	8.3	30.4

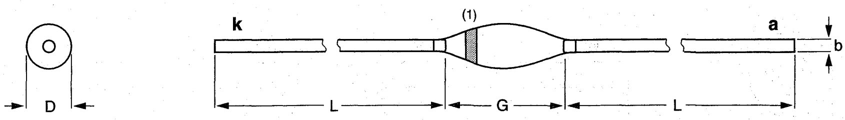
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61AC2						98-12-04

Package outlines

Hermetically sealed glass package; axial leaded; 2 leads — SOD61AD2



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

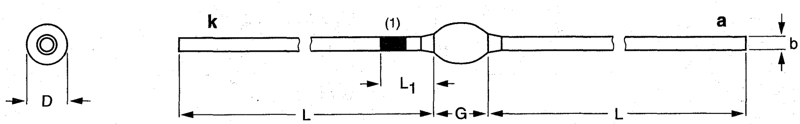
UNIT	b	D max.	G max.	L min.
mm	0.6	2.5	8.7	30.2

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61AD2						97-12-04

Miniature hermetically sealed glass package; axial leaded; 2 leads — SOD61H2



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.	L_1 max.
mm	0.6	2.2	3	32.5	3

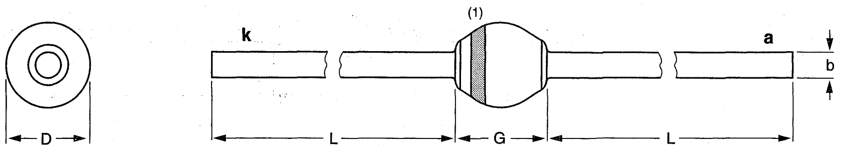
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD61H2						97-06-09

Package outlines — Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads — SOD64



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

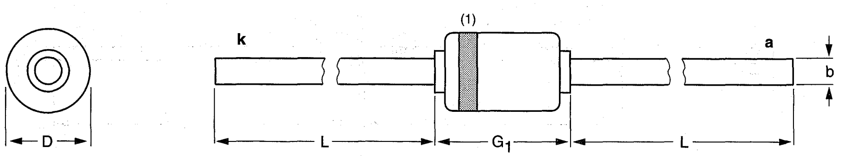
UNIT	b max.	D max.	G max.	L min.
mm	1.35	4.5	5.0	28

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD64						97-10-14

Hermetically sealed glass package; axial leaded; 2 leads — SOD66



0 2 4 mm
scale

DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G_1 max.	L min.
mm	0.81	2.6	4.8	28

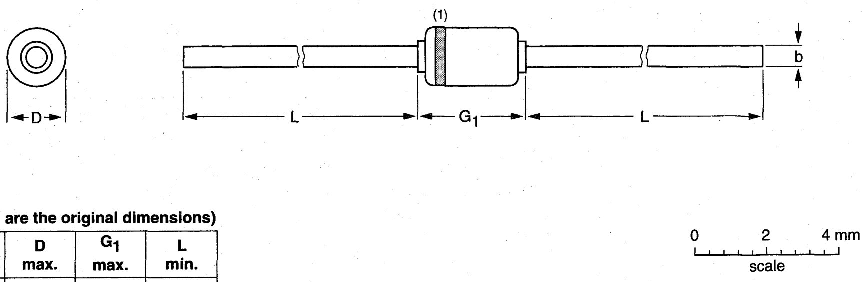
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD66		DO-41				97-06-20

Package outlines Chapter 2

Hermetically sealed glass package; axial leaded; 2 leads SOD68

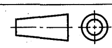


DIMENSIONS (mm are the original dimensions)

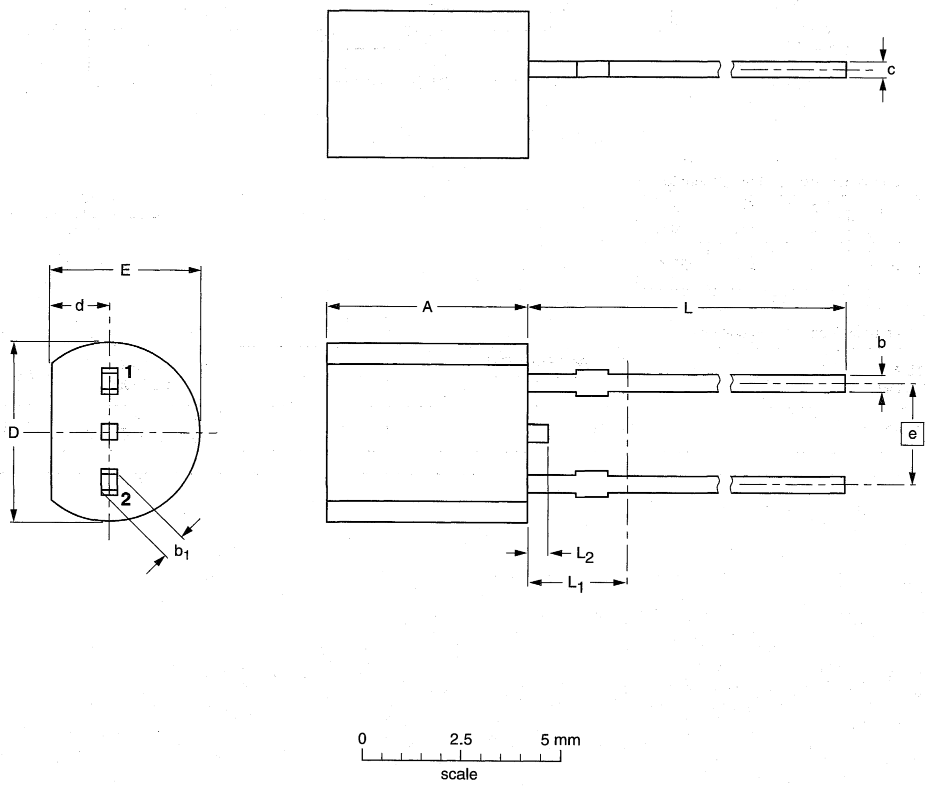
UNIT	b max.	D max.	G_1 max.	L min.
mm	0.55	1.6	3.04	25.4

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD68		DO-34				97-06-09

Plastic near cylindrical single-ended package; 2 in-line leads **SOD70**



DIMENSIONS (mm are the original dimensions)

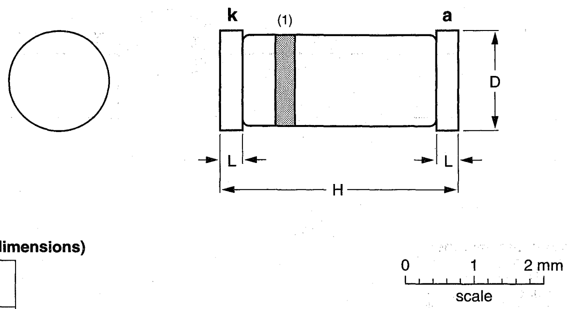
UNIT	A	b	b_1	c	D	d	E	e	L	L_1(1) max.	L_2
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	14.5 12.7	2.5	0.7 0.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD70						98-05-25

Hermetically sealed glass surface mounted package; 2 connectors SOD80C



DIMENSIONS (mm are the original dimensions)

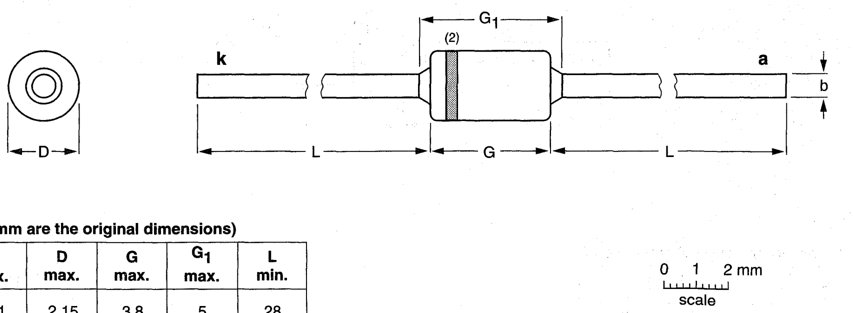
UNIT	D	H	L
mm	1.60 1.45	3.7 3.3	0.3

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD80C	100H01					97-06-20

Hermetically sealed glass package; Implotec$^{TM(1)}$ technology; axial leaded; 2 leads SOD81



DIMENSIONS (mm are the original dimensions)

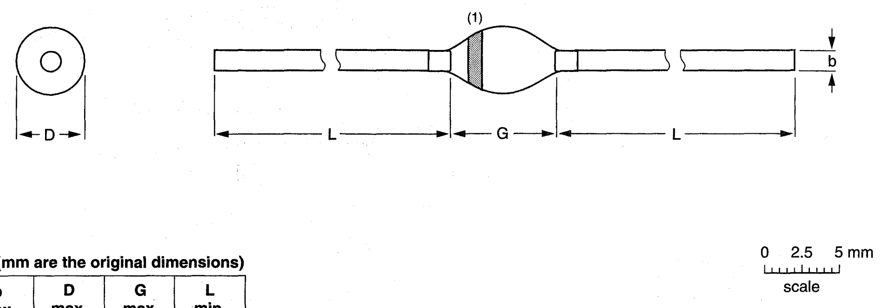
UNIT	b max.	D max.	G max.	G_1 max.	L min.
mm	0.81	2.15	3.8	5	28

Notes

1. Implotec is a trademark of Philips.
2. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD81						97-06-20

Hermetically sealed glass package; axial leaded; 2 leads SOD83A



DIMENSIONS (mm are the original dimensions)

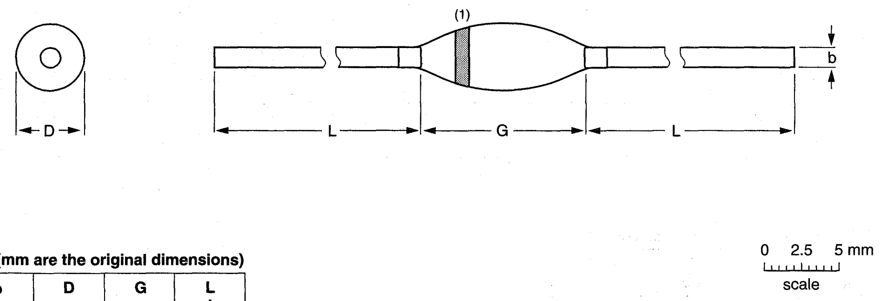
UNIT	b max.	D max.	G max.	L min.
mm	1.35	4.5	7.5	30.7

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD83A						97-06-11

Hermetically sealed glass package; axial leaded; 2 leads SOD83B



DIMENSIONS (mm are the original dimensions)

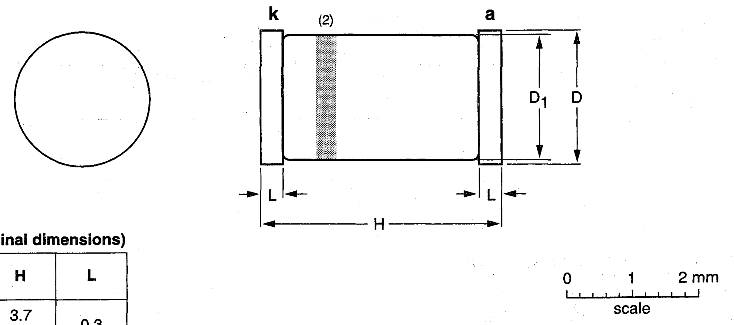
UNIT	b max.	D max.	G max.	L min.
mm	1.35	4.5	11	29

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD83B						97-06-27

Hermetically sealed glass surface mounted package; Implotec™(1) technology; 2 connectors — SOD87



DIMENSIONS (mm are the original dimensions)

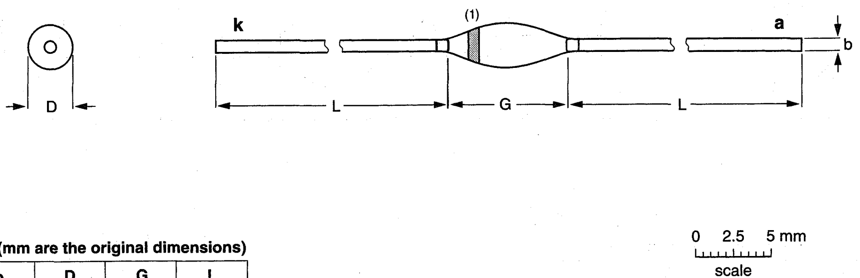
UNIT	D	D1	H	L
mm	2.1 2.0	2.0 1.8	3.7 3.3	0.3

Notes

1. Implotec is a trademark of Philips.
2. The marking indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD87	100H03					99-03-31

Hermetically sealed glass package; axial leaded; 2 leads — SOD88A



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.8	8	30.5

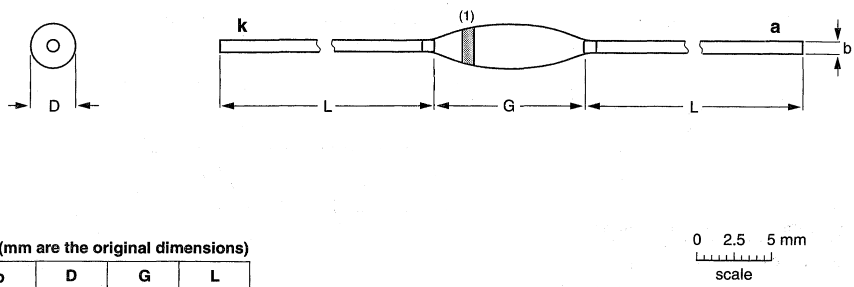
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD88A						97-06-20

Hermetically sealed glass package; axial leaded; 2 leads

SOD88B



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.
mm	0.81	3.8	11	29

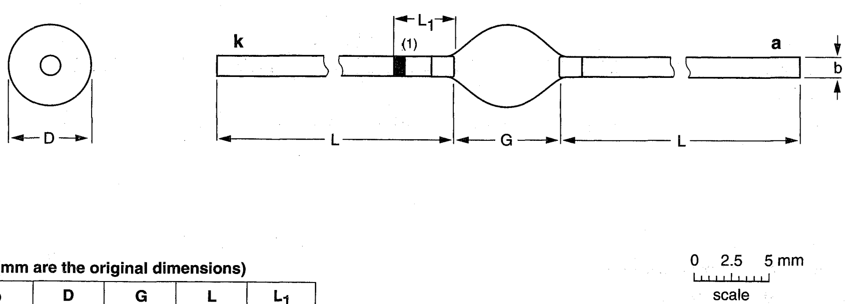
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD88B						97-06-20

Hermetically sealed glass package; axial leaded; 2 leads

SOD89A



DIMENSIONS (mm are the original dimensions)

UNIT	b max.	D max.	G max.	L min.	L_1 max.
mm	1.35	5.5	7	31	3

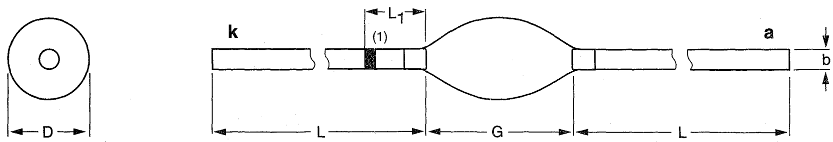
Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD89A						97-06-20

Package outlines

Hermetically sealed glass package; axial leaded; 2 leads — SOD89B



0 2.5 5 mm
scale

DIMENSIONS (mm are the original dimensions)

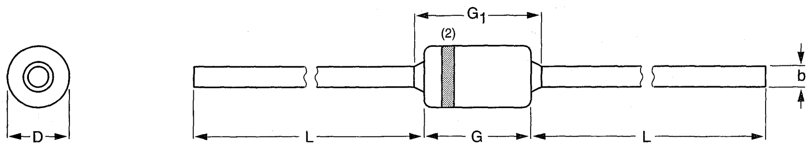
UNIT	b max.	D max.	G max.	L min.	L_1 max.
mm	1.35	5.5	10	29.5	3

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD89B						97-06-20

Hermetically sealed glass package; Implotec$^{TM(1)}$ technology; axial leaded; 2 leads — SOD91



0 1 2 mm
scale

DIMENSIONS (mm are the original dimensions)

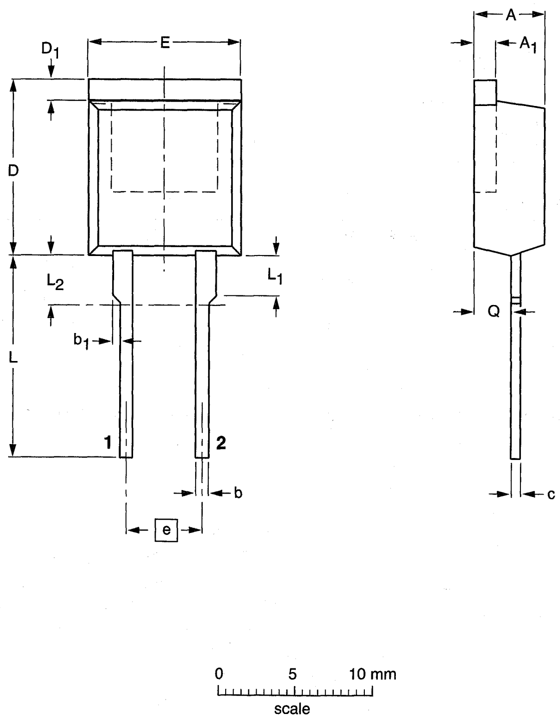
UNIT	b max.	D max.	G max.	G_1 max.	L min.
mm	0.55	1.7	3.0	3.5	29

Note

1. Implotec is a trademark of Philips.
2. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD91						97-06-09

Plastic single-ended package; 2-lead low-profile TO-220 SOD95



DIMENSIONS (mm are the original dimensions)

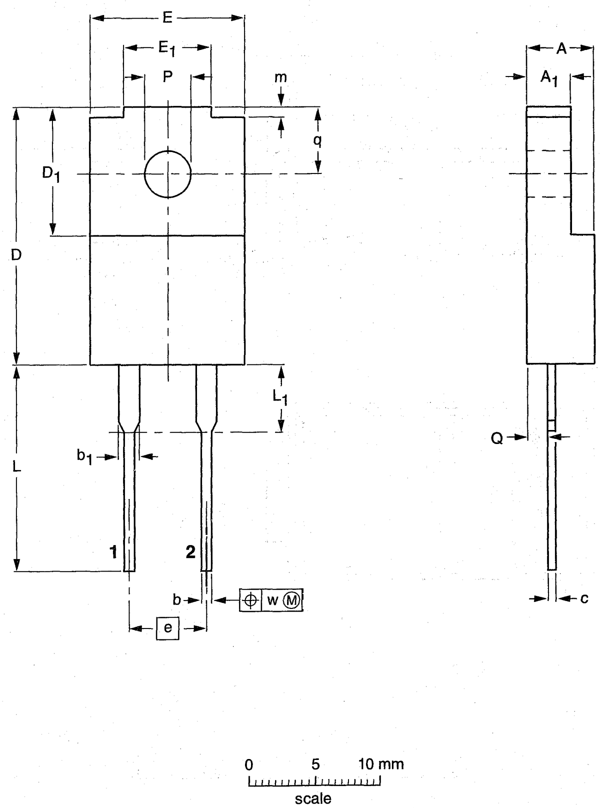
UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	L_2[(1)] max	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	5.08	15.0 13.5	3.30 2.79	3.0	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD95		low-profile 2-lead TO-220				97-06-11

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-lead TO-220F exposed tabs **SOD100**



DIMENSIONS (mm are the original dimensions)

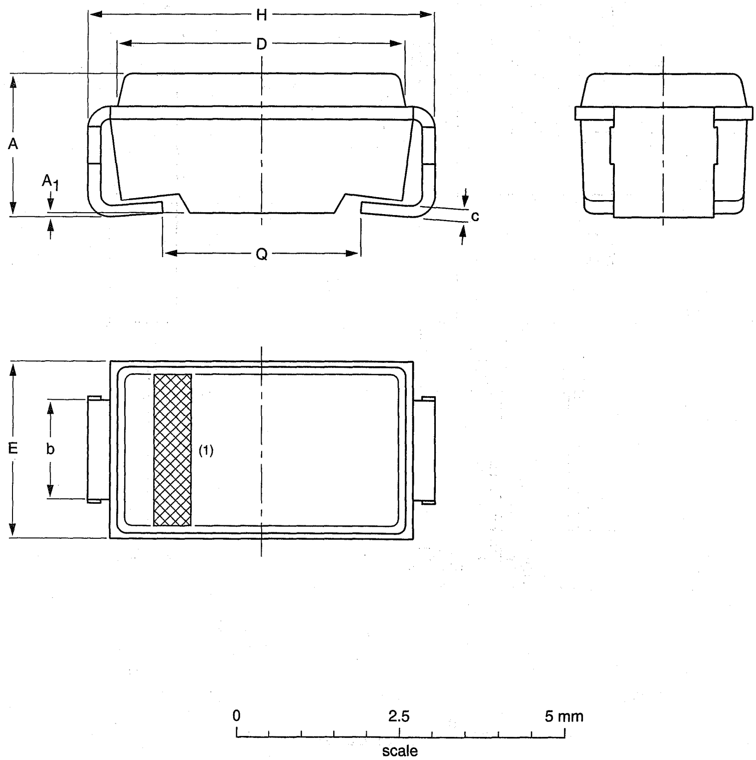
UNIT	A	A_1	b	b_1	c	D	D_1	E	E_1	e	L	$L_1^{(1)}$	m	P	Q	q	w
mm	4.4 4.0	2.9 2.5	0.9 0.7	1.5 1.3	0.55 0.38	17.0 16.4	7.9 7.5	10.2 9.6	5.7 5.3	5.08	14.3 13.5	4.8 4.0	0.9 0.5	3.2 3.0	1.4 1.2	4.4 4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD100		2-lead TO-220F				97-06-11

Transfer-moulded thermo-setting plastic small rectangular surface mounted package; 2 connectors **SOD106**



DIMENSIONS (mm are the original dimensions)

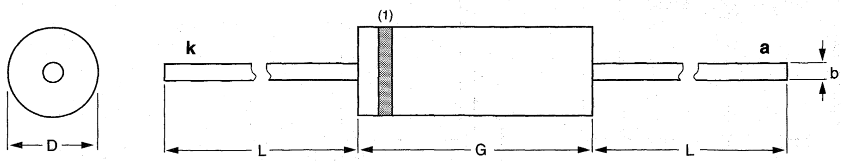
UNIT	A	A_1	b	c	D	E	H	Q
mm	2.3 2.0	0.05	1.6 1.4	0.2	4.5 4.3	2.8 2.4	5.5 5.1	3.3 2.7

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD106		DO-214AC				97-06-09

Hermetically sealed plastic package; axial leaded; 2 leads SOD107A



DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.6	3.1 2.9	8.5 7.5	30

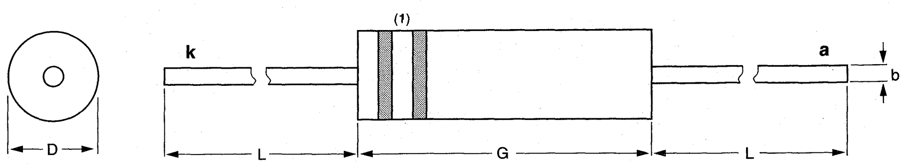
0 2.5 5 mm
scale

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD107A						98-08-04

Hermetically sealed plastic package; axial leaded; 2 leads SOD107B



DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.6	3.1 2.9	10.5 9.5	29

0 2.5 5 mm
scale

Note

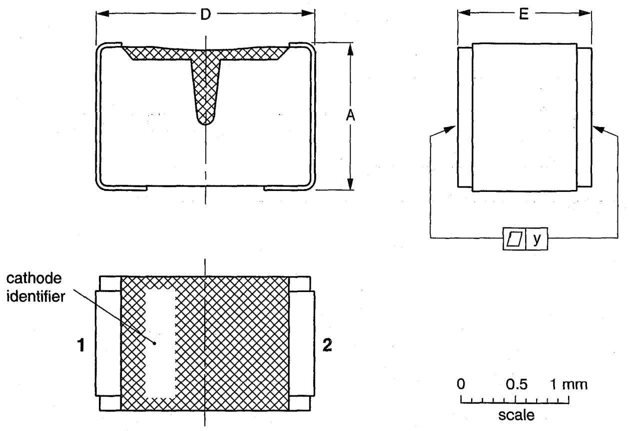
1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD107B						98-08-05

Package outlines

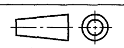
Chapter 2

Very small ceramic rectangular surface mounted package **SOD110**

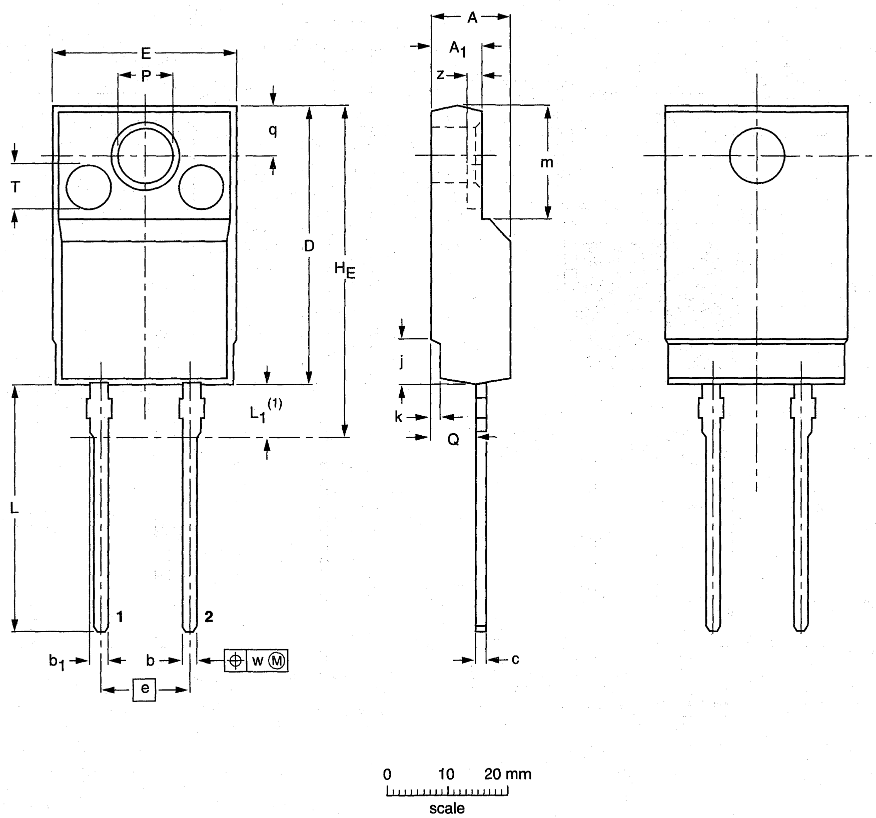


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	D	E	y
mm	1.6	2.10 1.90	1.40 1.10	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD110						97-04-14

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 2-lead TO-220 'full pack' **SOD113**



DIMENSIONS (mm are the original dimensions)

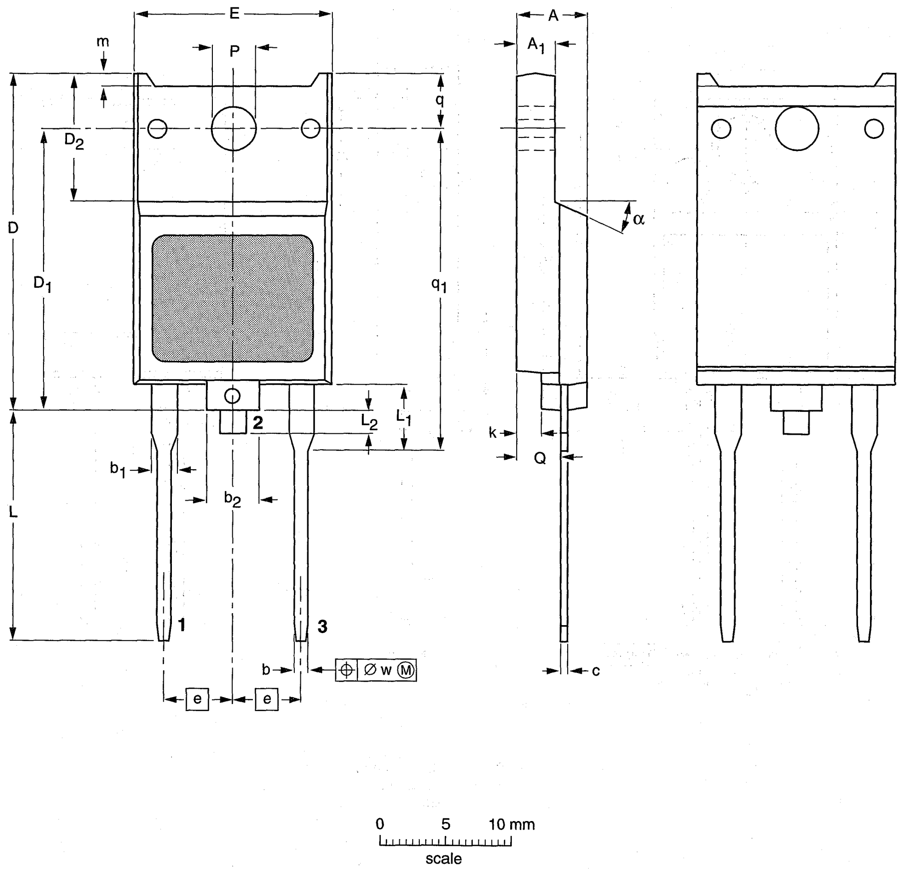
UNIT	A	A_1	b	b_1	c	D	E	e	H_E max.	j	k	L	$L_1^{(1)}$	m	P	Q	q	T	w	$z^{(2)}$
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	0.7 0.4	15.8 15.2	10.3 9.7	5.08	19.0	2.7 2.3	0.6 0.4	14.4 13.5	3.3 2.8	6.5 6.3	3.2 3.0	2.6 2.3	2.6	2.55	0.4	0.8

Notes

1. Terminals are uncontrolled within zone L_1.
2. z is depth of T.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD113		2-lead TO-220				97-06-11

Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads (one lead cropped) **SOD117**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	b_2	c	D	D_1	D_2	E	e	k	L	$L_1^{(1)}$	L_2	m	P	Q	q	q_1	w	α
mm	5.8	3.3	1.2	2.2	4.7	0.9	27	22.5	10.2	16	5.45	2.2	19.1	5.4	3.0	0.8	3.4	3.4	4.7	25.7	0.4	27°
	4.8	2.7	0.9	1.8	4.2	0.6	26	21.5	9.9	15		1.8	18.1	4.8	1.0	0.6	3.1	3.2	4.3	25.1		23°

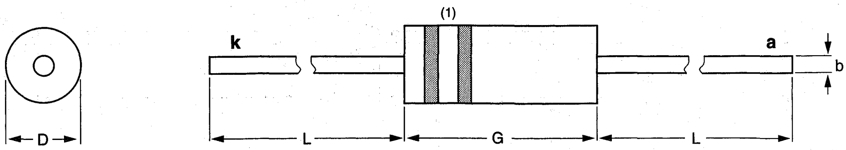
Note

1. Tinning of terminals are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD117						98-11-06

Package outlines | Chapter 2

Hermetically sealed plastic package; axial leaded; 2 leads — SOD118A



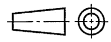
DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.5	2.6 2.4	6.7 6.3	31

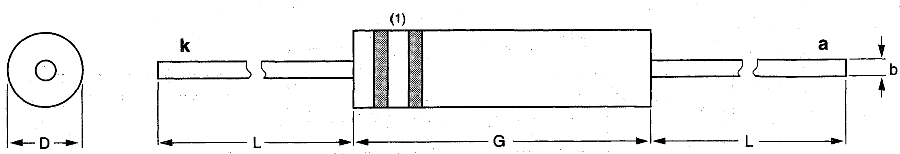
0 2.5 5 mm
scale

Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD118A						98-05-28

Hermetically sealed plastic package; axial leaded; 2 leads — SOD118B



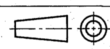
DIMENSIONS (mm are the original dimensions)

UNIT	b	D	G	L min.
mm	0.5	2.6 2.4	10.5 9.5	29

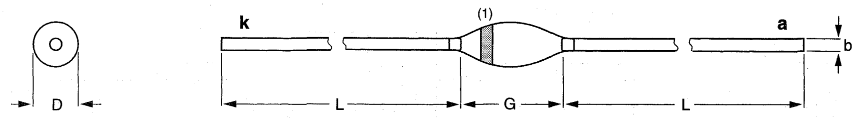
0 2.5 5 mm
scale

Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD118B						98-05-28

Hermetically sealed glass package; axial leaded; 2 leads **SOD119AB**



DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G max.	L min.
mm	0.8	2.5	5.5	31.8

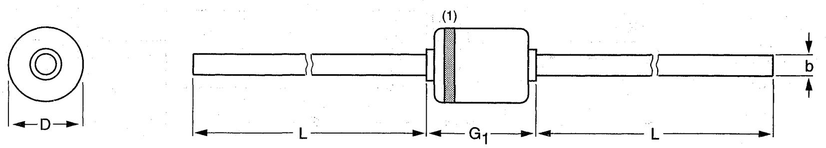
0 2.5 5 mm
scale

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD119AB						98-12-04

Hermetically sealed glass package; axial leaded; 2 leads **SOD120**



DIMENSIONS (mm are the original dimensions)

UNIT	b	D max.	G_1 max.	L min.
mm	0.6	2.15	3.0	28

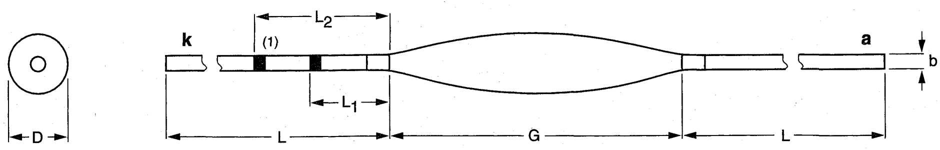
0 2 4 mm
scale

Note

1. The marking band indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD120						98-05-25

Hermetically sealed glass package; axial leaded; 2 leads SOD121AB to AJ

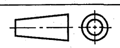


DIMENSIONS (mm are the original dimensions)

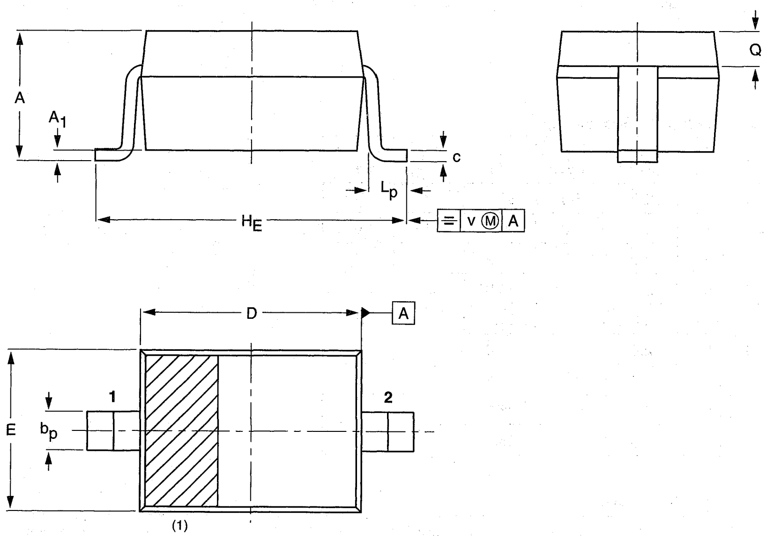
OUTLINE VERSION	b	D max.	G max.	L min.	L_1 max.	L_2 max.
SOD121AB	0.5	2.0	5.5	31.8	3	5
SOD121AC	0.5	2.0	8.3	30.4	3	5
SOD121AD	0.5	2.0	8.7	30.2	3	5
SOD121AE	0.5	2.0	9.1	30.0	3	5
SOD121AF	0.5	2.0	9.5	29.8	3	5
SOD121AG	0.5	2.0	9.9	29.6	3	5
SOD121AH	0.5	2.0	10.5	29.3	3	5
SOD121AI	0.5	2.0	11.5	28.8	3	5
SOD121AJ	0.5	2.0	12.5	28.3	3	5

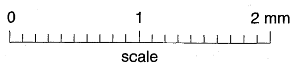
Note

1. The marking bands indicate the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD121AB to AJ						99-01-28

Plastic surface mounted package; 2 leads **SOD323**



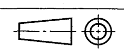


DIMENSIONS (mm are the original dimensions)

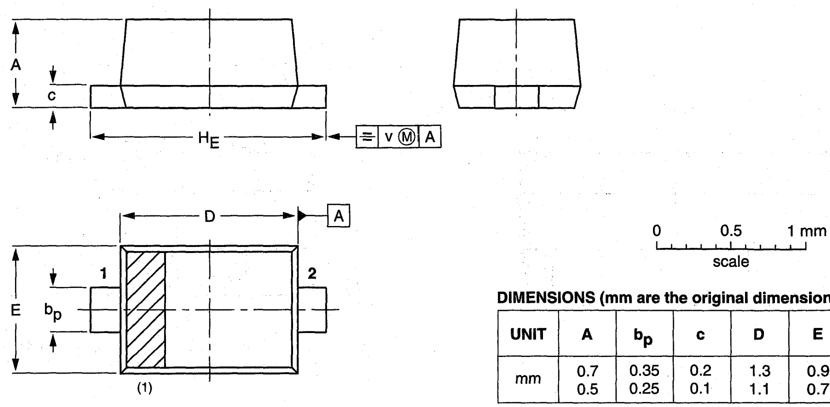
UNIT	A	A_1 max.	b_p	c	D	E	H_E	L_p	Q	v
mm	1.1 0.8	+ 0.05 − 0.05	0.40 0.25	0.25 0.10	1.8 1.6	1.35 1.15	2.7 2.3	0.45 0.15	0.25 0.15	0.2

Note

1. The marking bar indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD323						98-09-14

Plastic surface mounted package; 2 leads **SOD523**

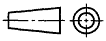


DIMENSIONS (mm are the original dimensions)

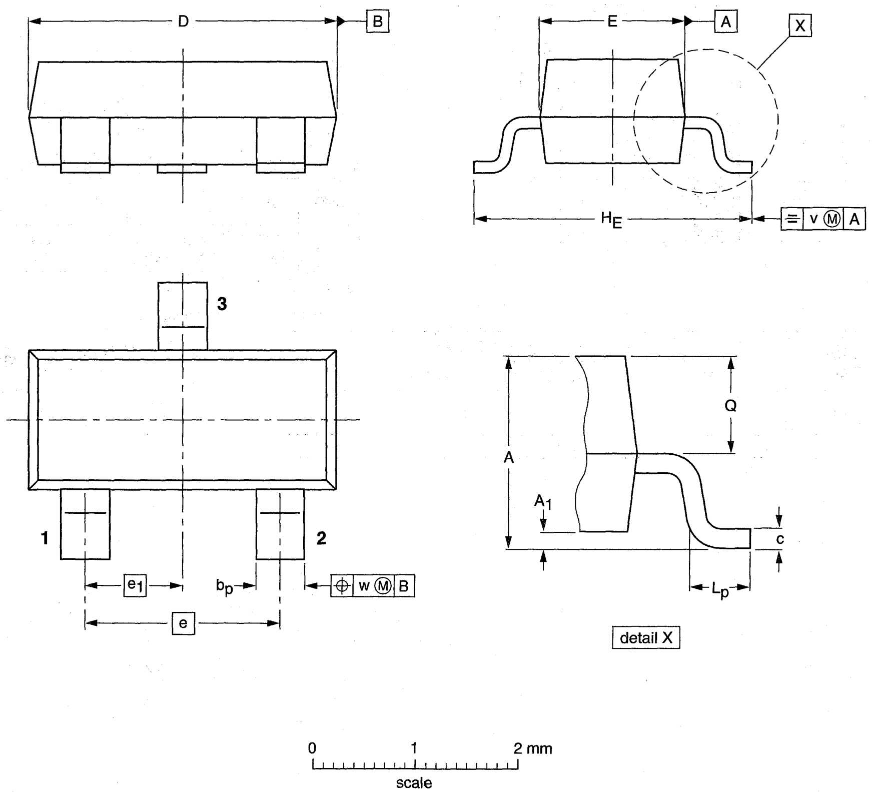
UNIT	A	b_p	c	D	E	H_E	v
mm	0.7 0.5	0.35 0.25	0.2 0.1	1.3 1.1	0.9 0.7	1.7 1.5	0.15

Note

1. The marking bar indicates the cathode.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOD523			SC-79			98-11-25

Plastic surface mounted package; 3 leads **SOT23**

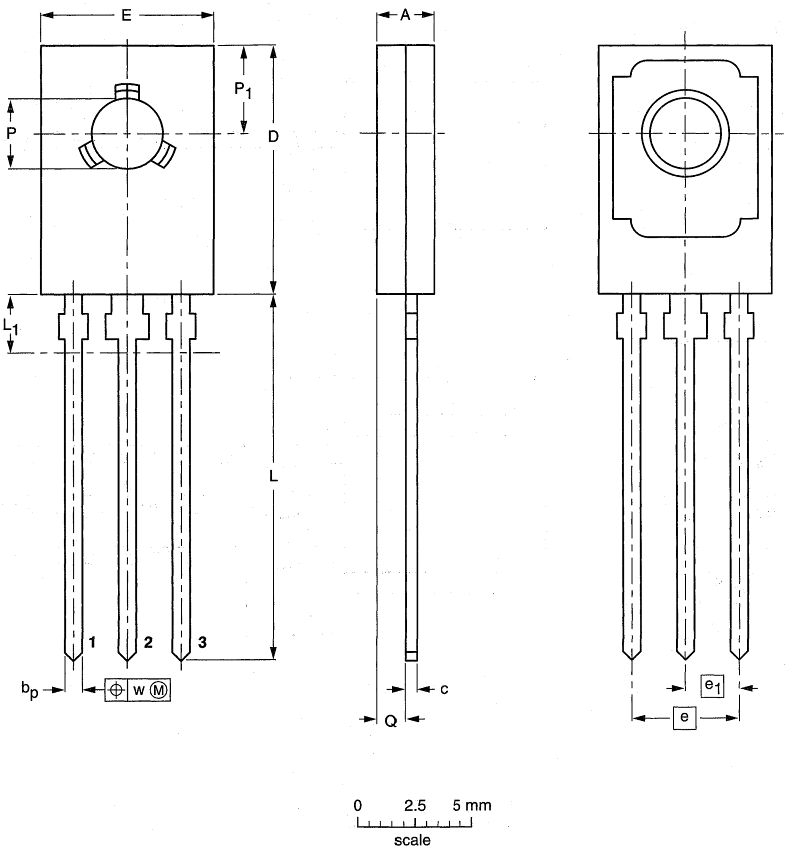


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max.	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.9	0.1	0.48 0.38	0.15 0.09	3.0 2.8	1.4 1.2	1.9	0.95	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT23						97-02-28

Plastic single-ended leaded (through hole) package; mountable to heatsink, 1 mounting hole; 3 leads SOT32



DIMENSIONS (mm are the original dimensions)

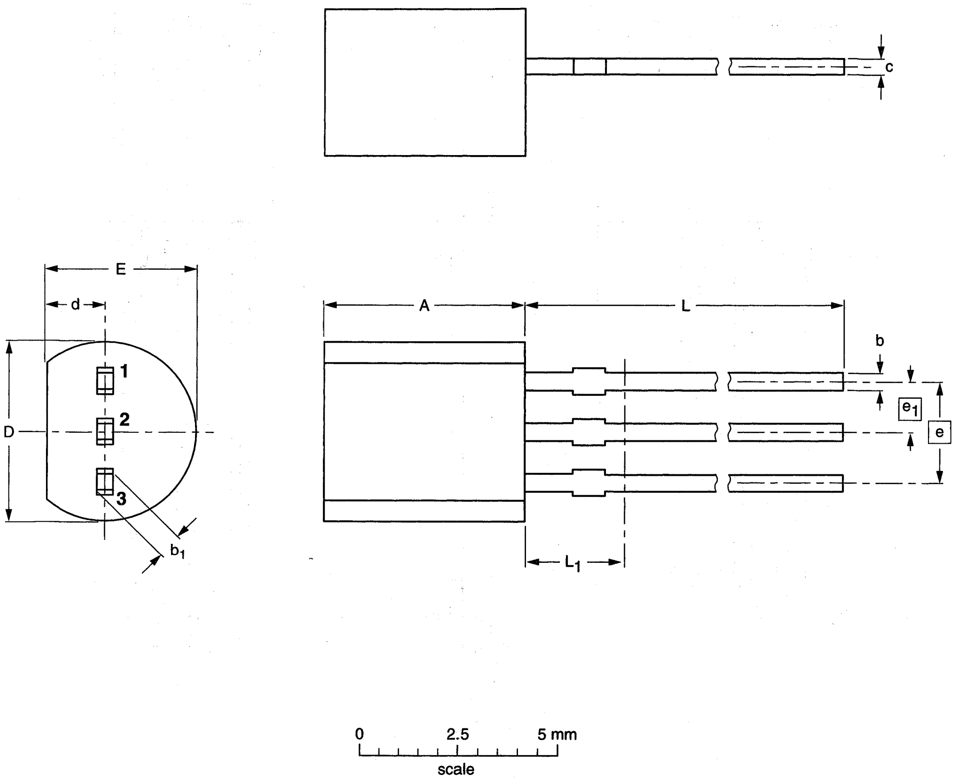
UNIT	A	b_p	c	D	E	e	e_1	L	L_1(1) max	Q	P	P_1	w
mm	2.7 2.3	0.88 0.65	0.60 0.45	11.1 10.5	7.8 7.2	4.58	2.29	16.5 15.3	2.54	1.5 0.9	3.2 3.0	3.9 3.6	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT32		TO-126				97-03-04

Plastic single-ended leaded (through hole) package; 3 leads **SOT54**

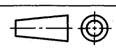


DIMENSIONS (mm are the original dimensions)

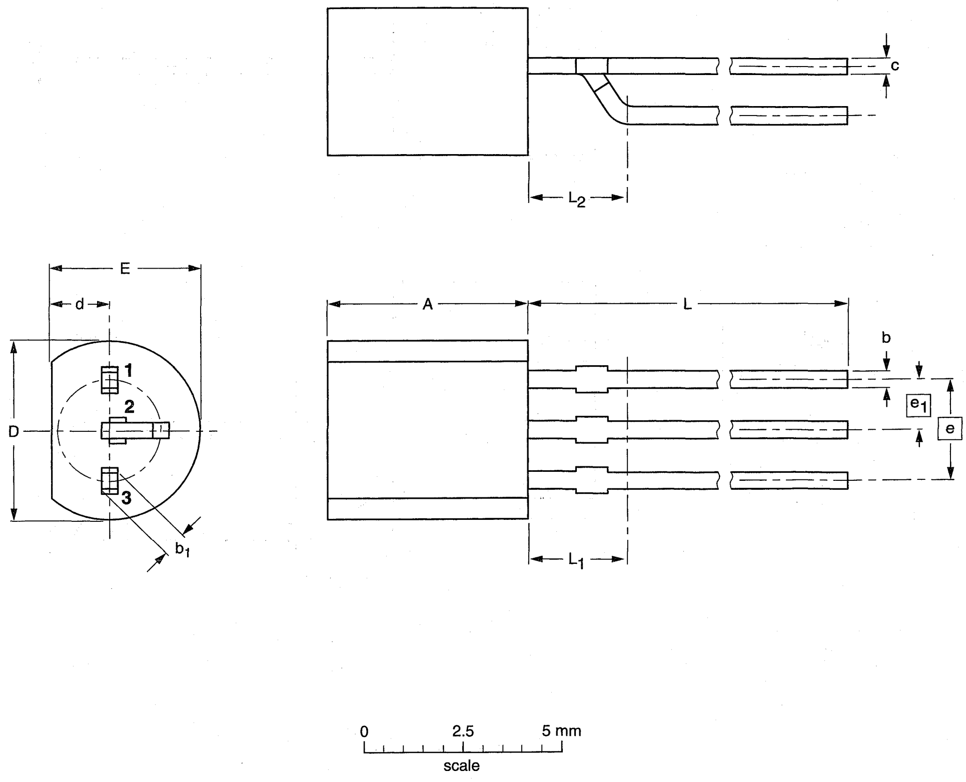
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	L_1(1)
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5

Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54		TO-92	SC-43			97-02-28

Plastic single-ended leaded (through hole) package; 3 leads (on-circle) **SOT54 variant**



DIMENSIONS (mm are the original dimensions)

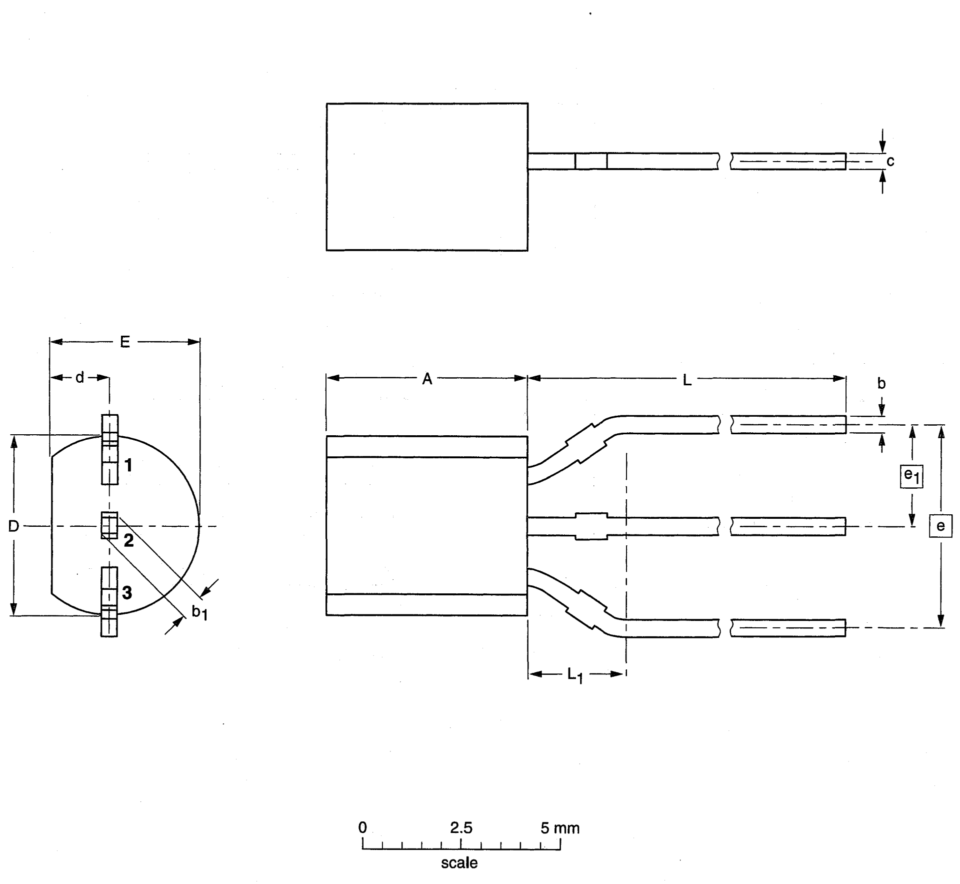
UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$ max	L_2 max
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	2.54	1.27	14.5 12.7	2.5	2.5

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54 variant		TO-92 variant	SC-43			98-03-26

Plastic single-ended leaded (through hole) package; 3 leads (wide pitch) **SOT54A**



DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	c	D	d	E	e	e_1	L	$L_1^{(1)}$
mm	5.2 5.0	0.48 0.40	0.66 0.56	0.45 0.40	4.8 4.4	1.7 1.4	4.2 3.6	5.08	2.54	14.5 12.7	2.5

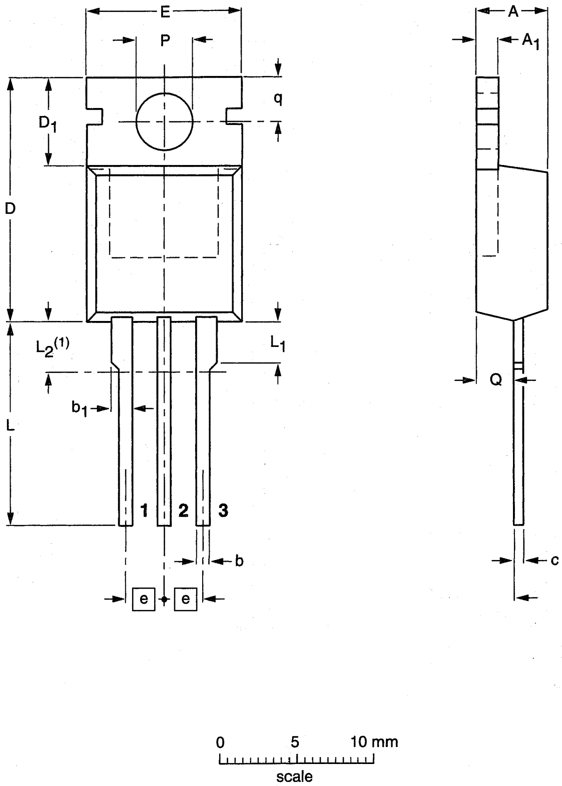
Note

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT54A		TO-92	SC-43			97-05-13

Package outlines Chapter 2

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

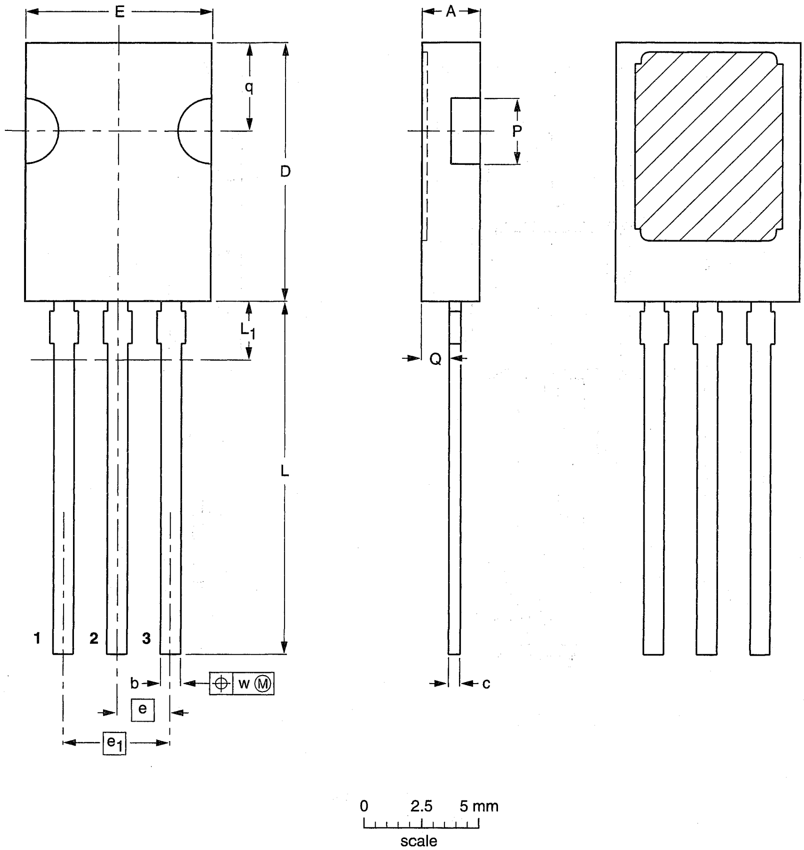
UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	$L_2^{(1)}$ max.	P	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		TO-220AB				97-06-11

Plastic single-ended package; 3 leads (in-line) **SOT82**

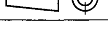


DIMENSIONS (mm are the original dimensions)

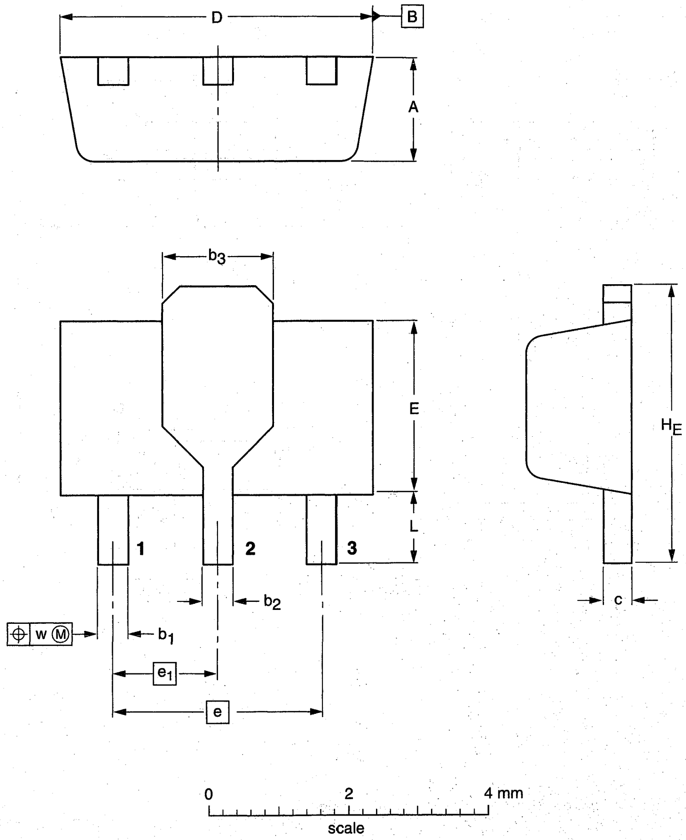
UNIT	A	b	c	D	E	e	e_1	L	$L_1^{(1)}$ max.	P	Q	q	w
mm	2.8 2.3	0.88 0.65	0.58 0.47	11.1 10.5	7.8 7.2	2.29	4.58	16.5 15.3	2.54	3.1 2.5	1.5 0.9	3.9 3.5	0.254

Note

1. Terminal dimensions within this zone are uncontrolled to allow for body and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT82						97-06-11

Plastic surface mounted package; collector pad for good heat transfer; 3 leads **SOT89**

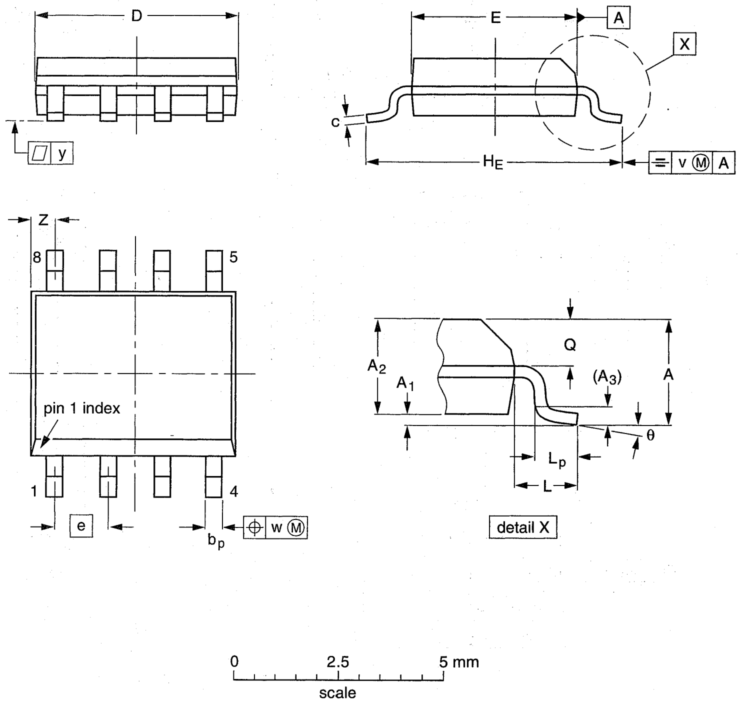


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_1	b_2	b_3	c	D	E	e	e_1	H_E	L min.	w
mm	1.6 1.4	0.48 0.35	0.53 0.40	1.8 1.4	0.44 0.37	4.6 4.4	2.6 2.4	3.0	1.5	4.25 3.75	0.8	0.13

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT89						97-02-28

SO8: plastic small outline package; 8 leads; body width 3.9 mm **SOT96-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

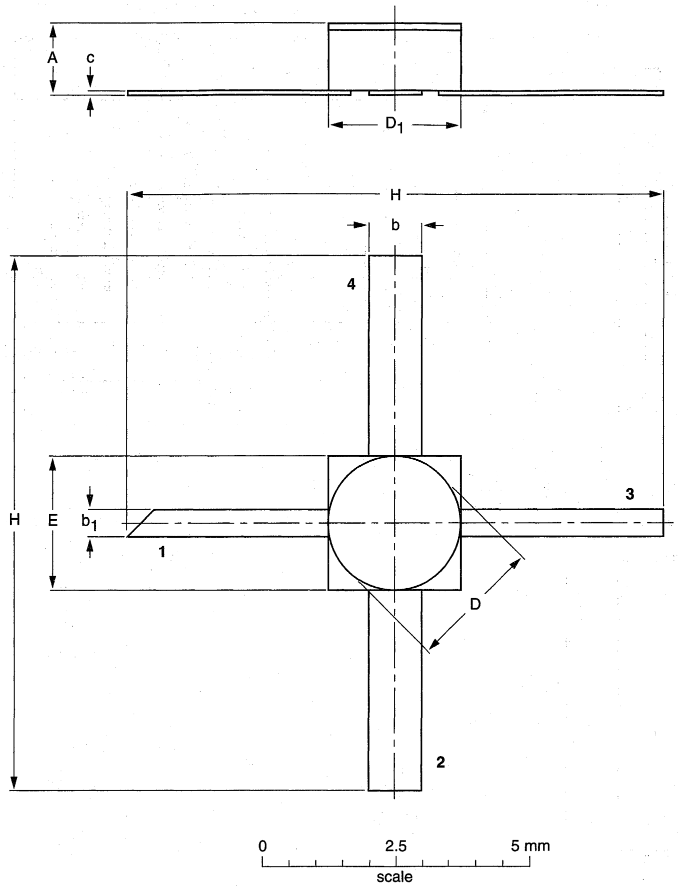
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	5.0 4.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.20 0.19	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.024	0.01	0.01	0.004	0.028 0.012	

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT96-1	076E03S	MS-012AA				~~95-02-04~~ 97-05-22

Surface mounted ceramic hermetic package; 4 leads **SOT100A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

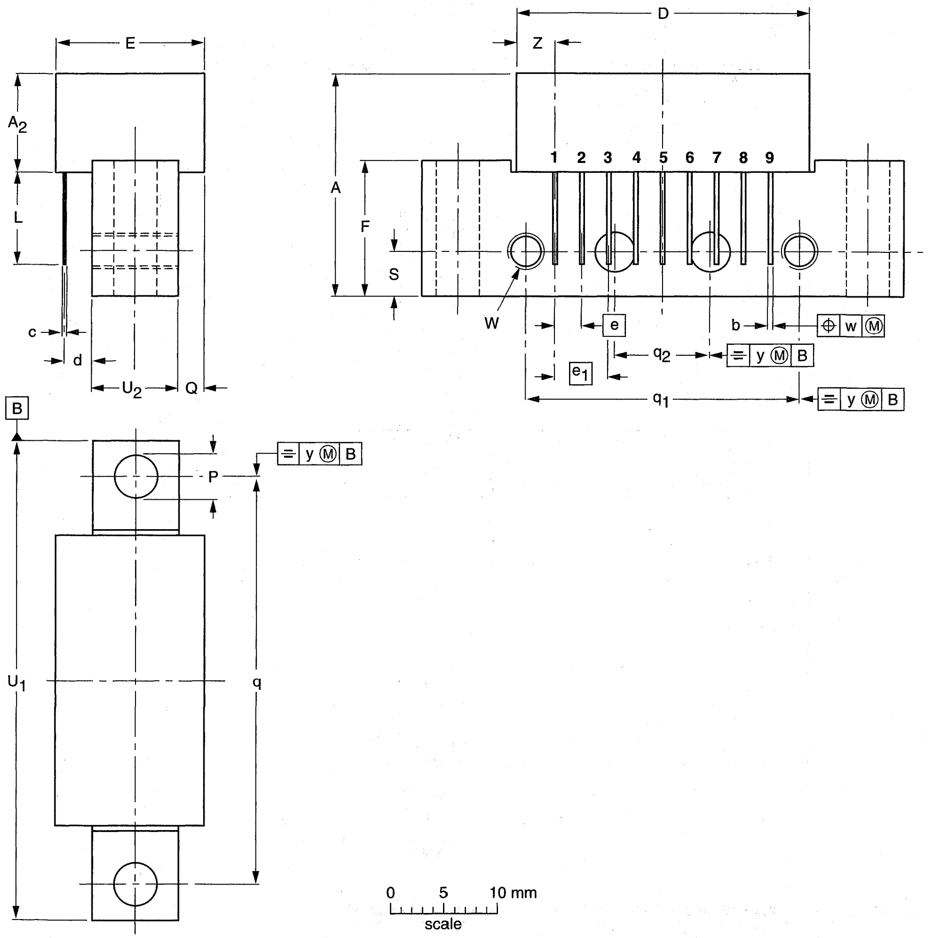
UNIT	A	b	b_1	c	D	D_1	E	H
mm	1.31 0.81	1.07 0.96	0.56 0.45	0.16 0.07	2.60 2.40	2.64 2.34	2.64 2.34	9.98 9.83
inches	0.052 0.032	0.043 0.037	0.023 0.017	0.006 0.003	0.102 0.094	0.104 0.092	0.104 0.092	0.393 0.387

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT100A						99-03-29

Package outlines

Chapter 2

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 9 gold-plated in-line leads **SOT115D**

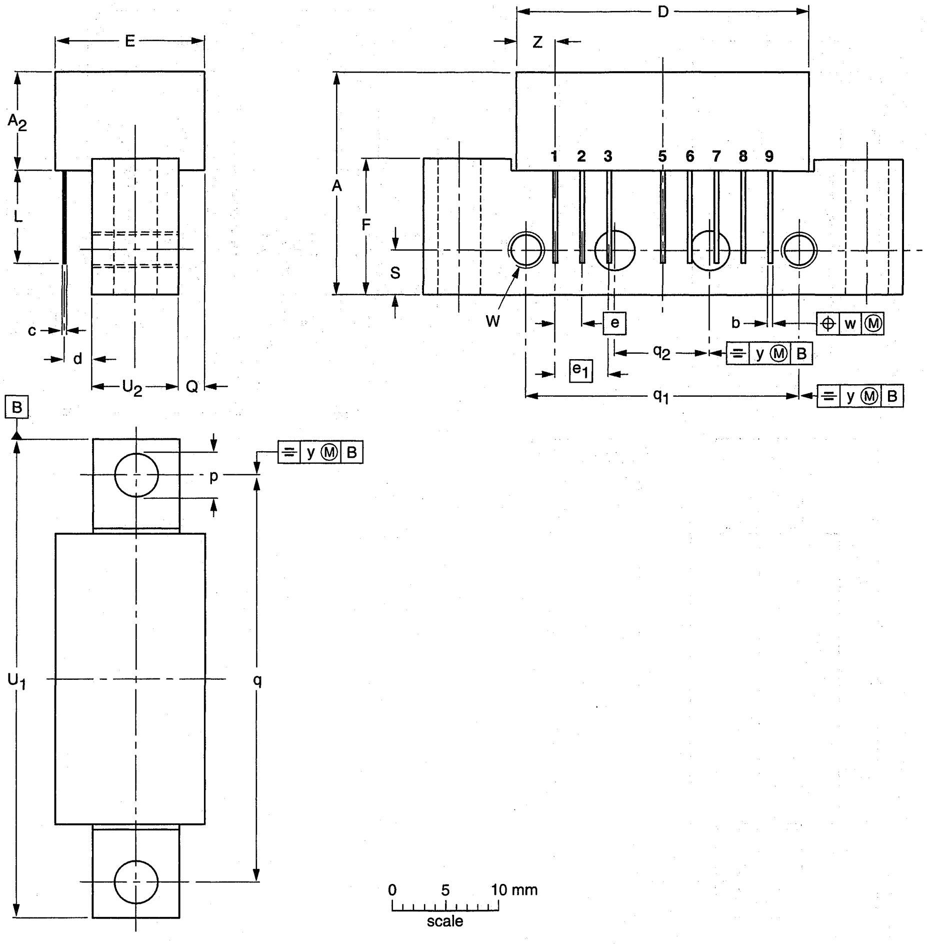


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	∅P	Q max.	q	q_1	q_2	S	U_1 max.	U_2	W	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115D						97-04-10

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 8 gold-plated in-line leads **SOT115G**

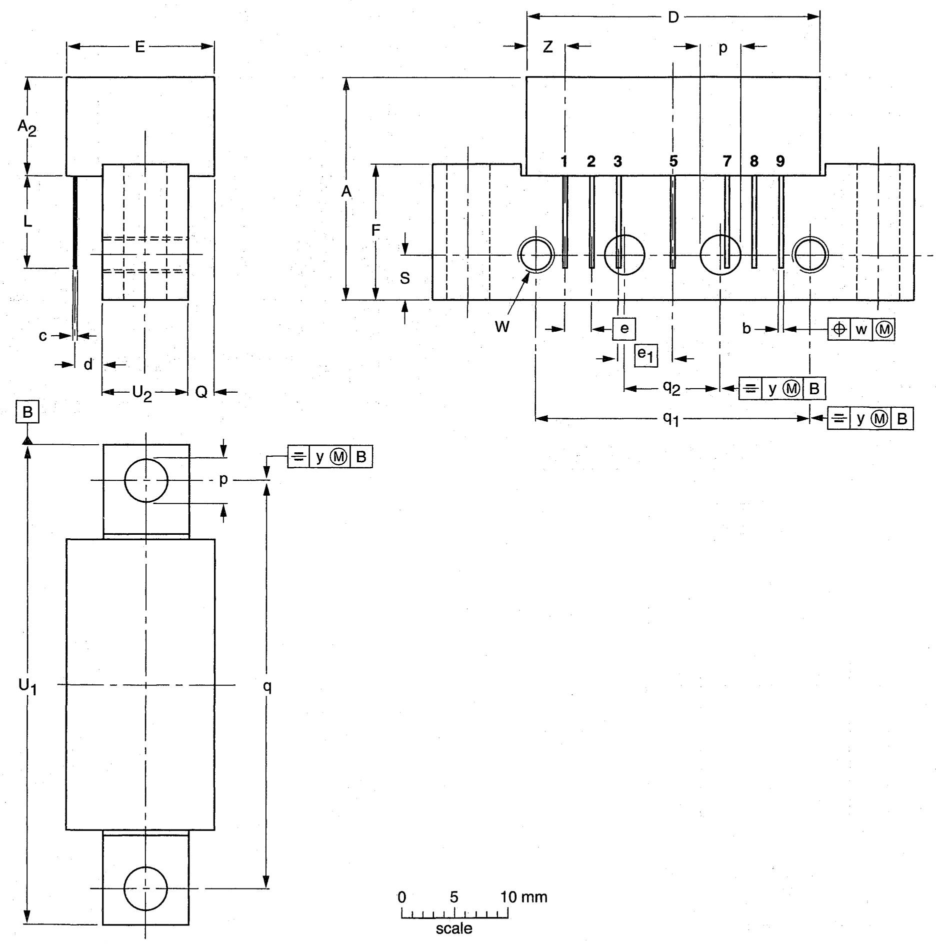


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	p	Q max.	q	q_1	q_2	S	U_1 max.	U_2	W	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115G						99-04-13

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; 7 gold-plated in-line leads **SOT115J**

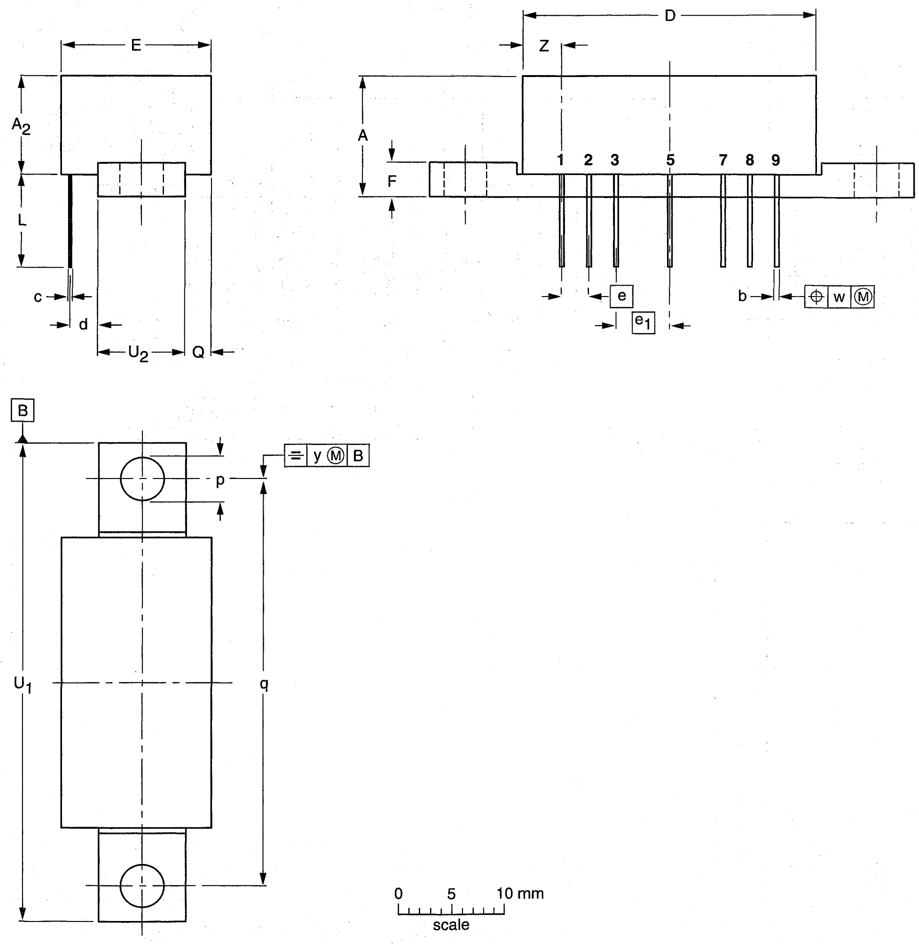


DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	p	Q max.	q	q_1	q_2	S	U_1 max.	U_2	W	w	y	Z max.
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	4.15 3.85	2.4	38.1	25.4	10.2	4.2	44.75	8	6-32 UNC	0.25	0.1	3.8

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115J						99-02-06

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 7 gold-plated in-line leads **SOT115L**



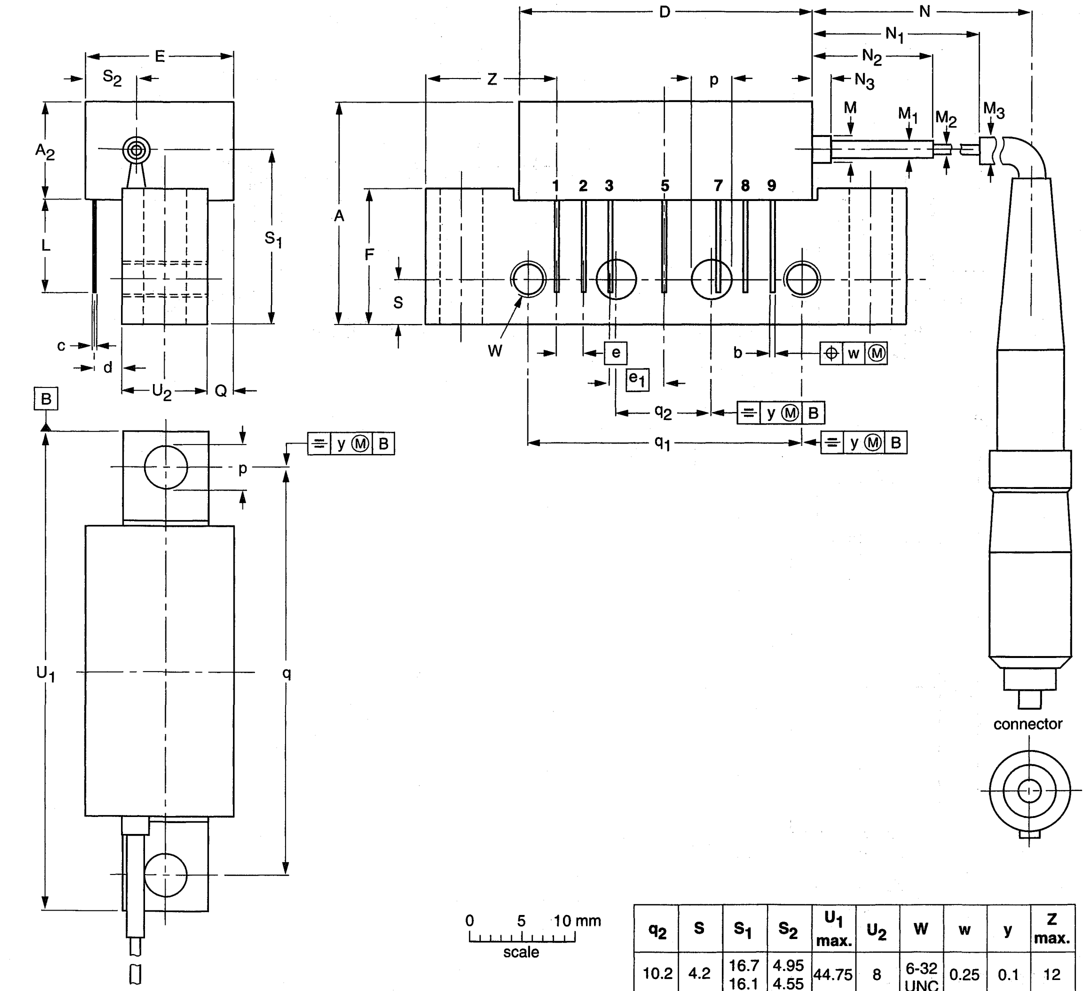
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	p	Q max.	q	U_1 max.	U_2	w	y	Z max.
mm	11.5	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	3.2	8.8	4.15 3.85	2.4	38.1	44.75	8	0.25	0.1	3.8

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115L						99-02-06

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads

SOT115N



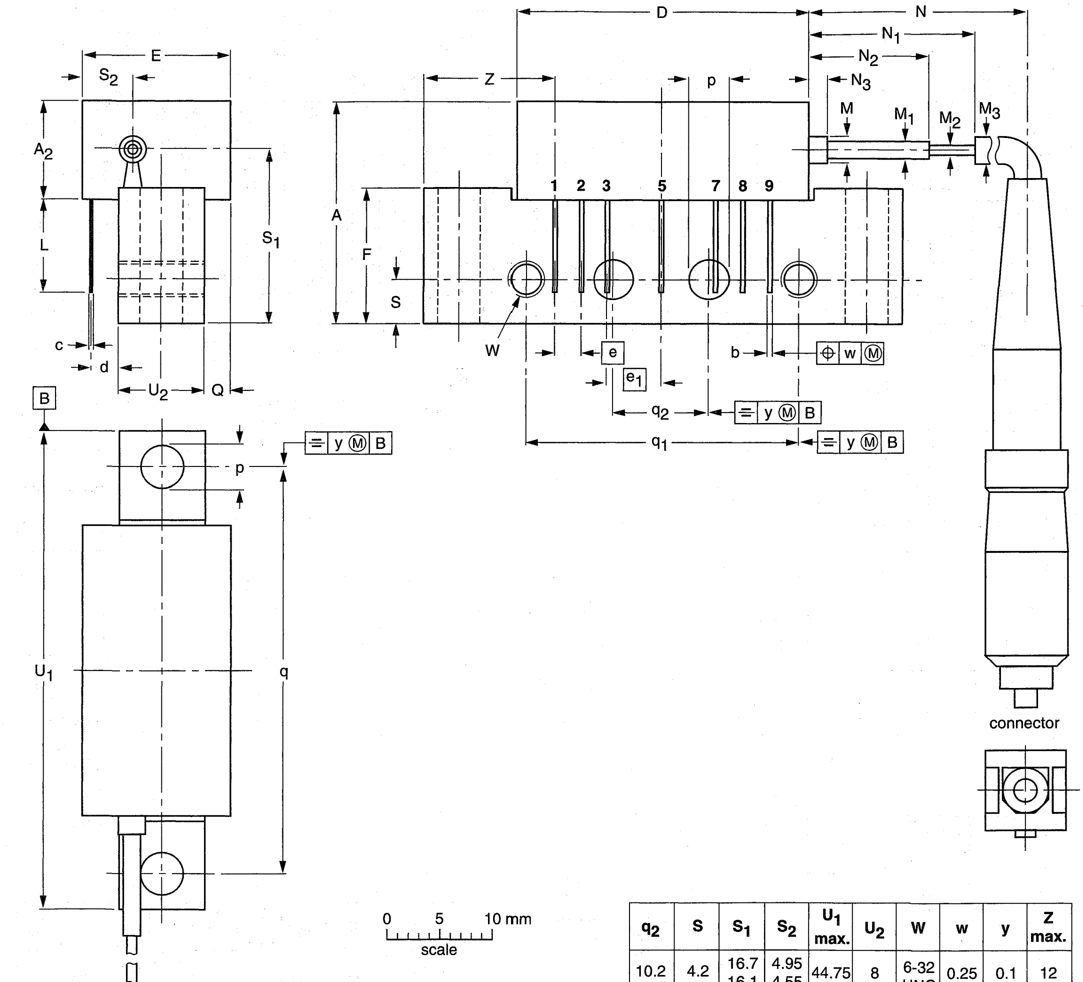
q2	S	S1	S2	U1 max.	U2	W	w	y	Z max.
10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A2 max.	b	c	D max.	d max.	E max.	e	e1	F	L min.	M	M1	M2	M3	N	N1	N2	N3	p	Q max.	q	q1
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	627 577	127 77	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115N						99-04-28

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads **SOT115P**



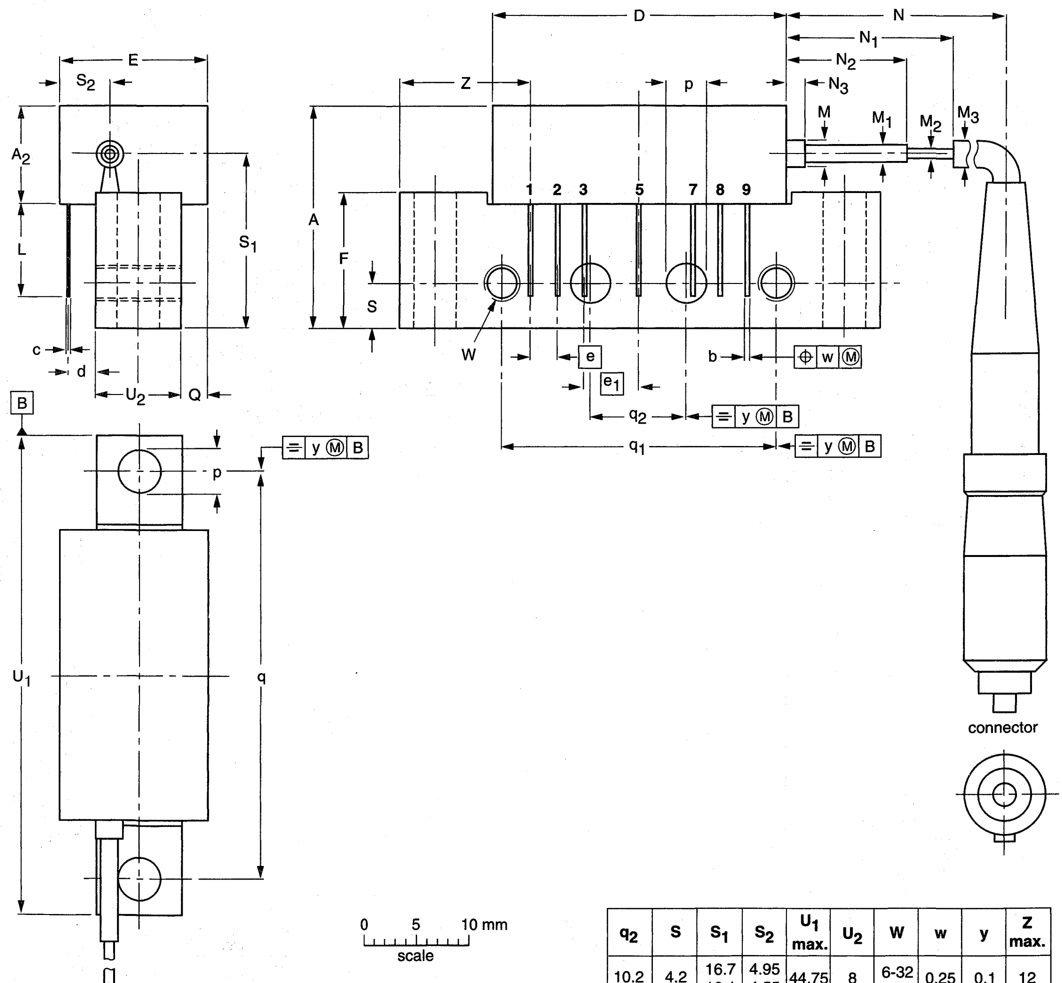
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	M	M_1	M_2	M_3	N	N_1	N_2	N_3	p	Q max.	q	q_1
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	917 817	15.3 8.7	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4

UNIT	q_2	S	S_1	S_2	U_1 max.	U_2	W	w	y	Z max.
mm	10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115P						99-02-06

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads **SOT115R**



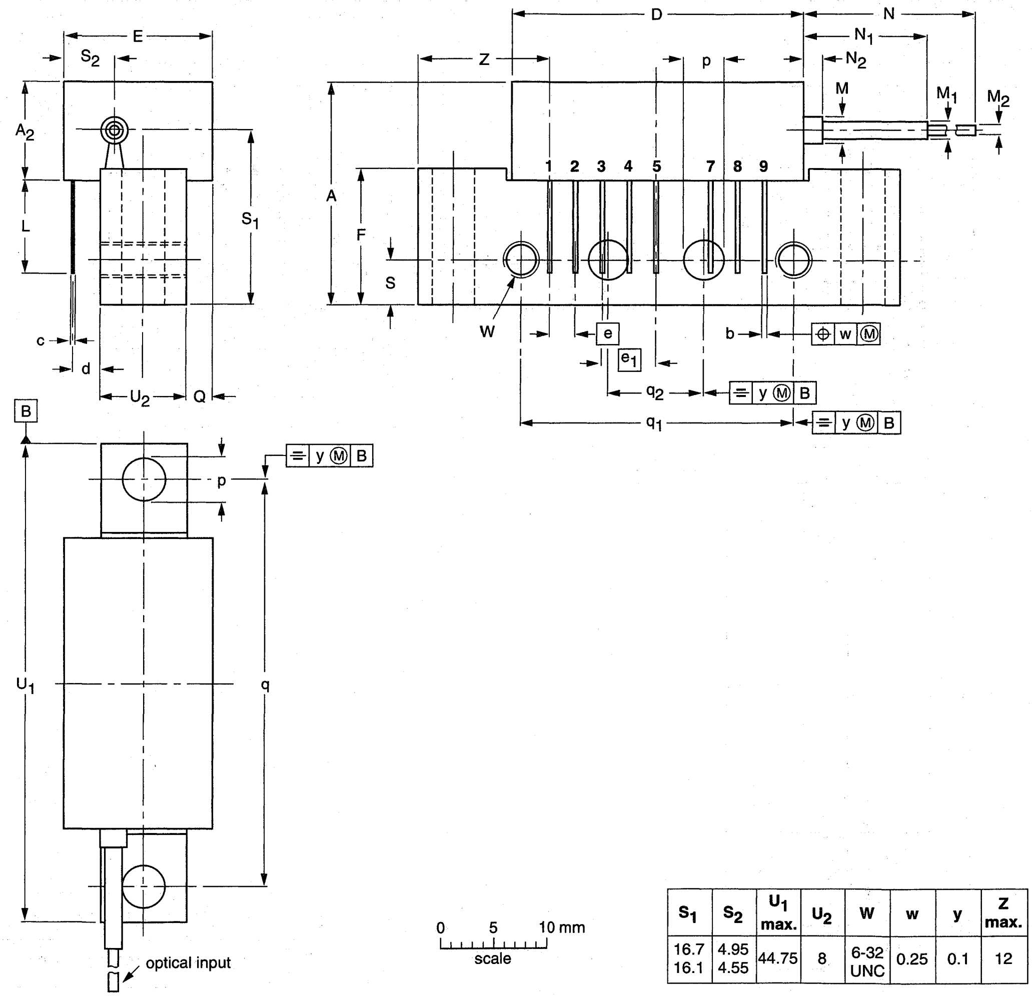
DIMENSIONS (mm are the original dimensions)

q2	S	S1	S2	U1 max.	U2	W	w	y	Z max.
10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

UNIT	A max.	A2 max.	b	c	D max.	d max.	E max.	e	e1	F	L min.	M	M1	M2	M3	N	N1	N2	N3	p	Q max.	q	q1
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	917 817	15.3 8.7	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115R						99-02-06

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 8 gold-plated in-line leads **SOT115T**



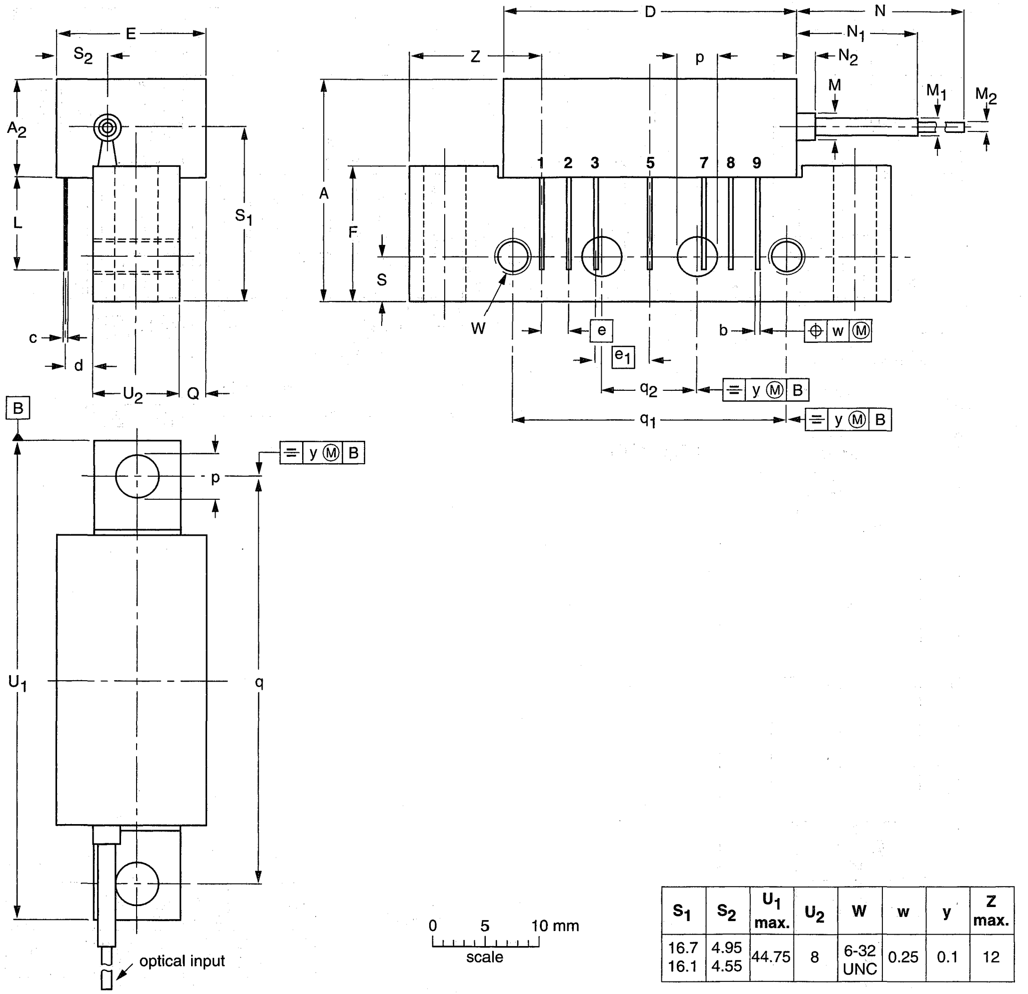
S_1	S_2	U_1 max.	U_2	W	w	y	Z max.
16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	M	M_1	M_2	N min.	N_1	N_2	p	Q max.	q	q_1	q_2	S
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	1000	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4	10.2	4.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115T						99-04-13

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input; 7 gold-plated in-line leads **SOT115U**



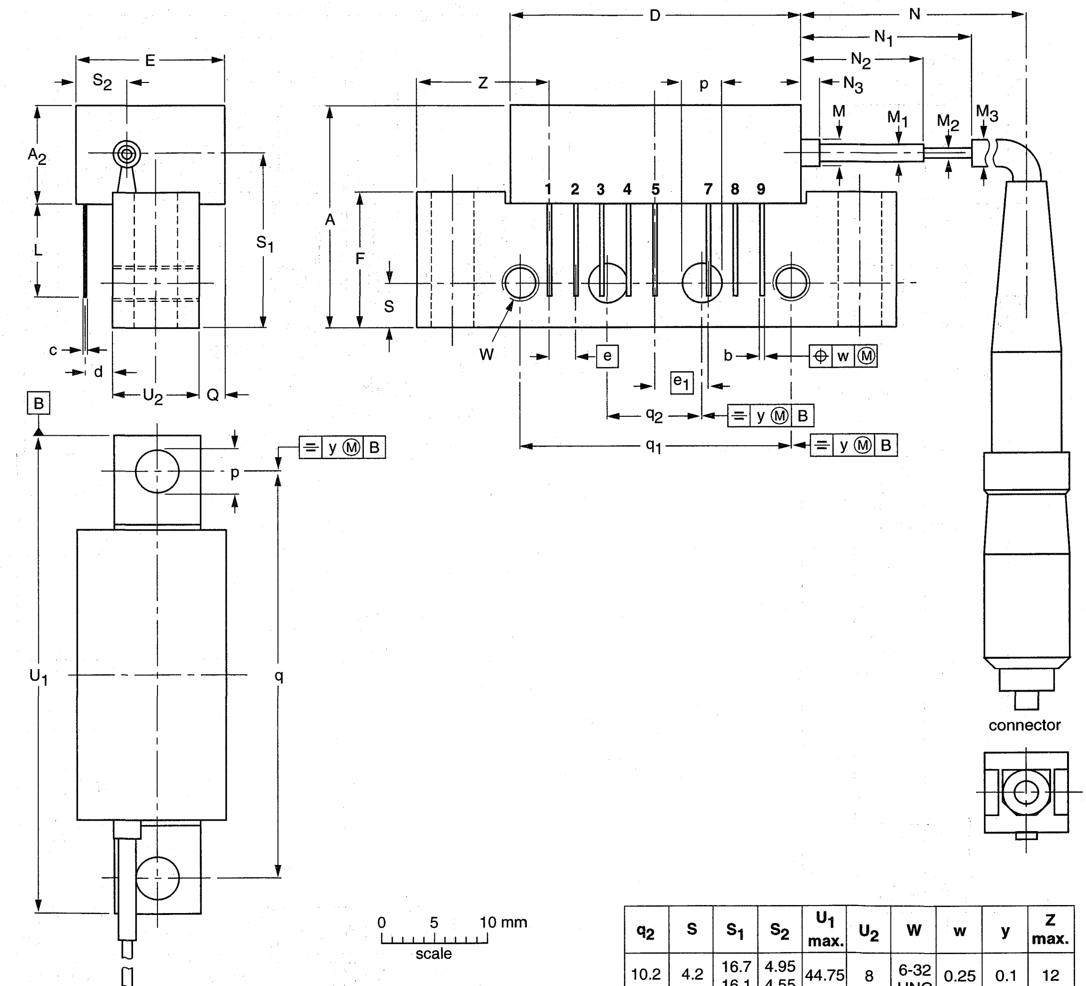
S_1	S_2	U_1 max.	U_2	W	w	y	Z max.
16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	M	M_1	M_2	N min.	N_1	N_2	p	Q max.	q	q_1	q_2	S
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	1000	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4	10.2	4.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115U						99-04-13

Rectangular single-ended package; aluminium flange; 2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes; optical input with connector; 7 gold-plated in-line leads **SOT115V**



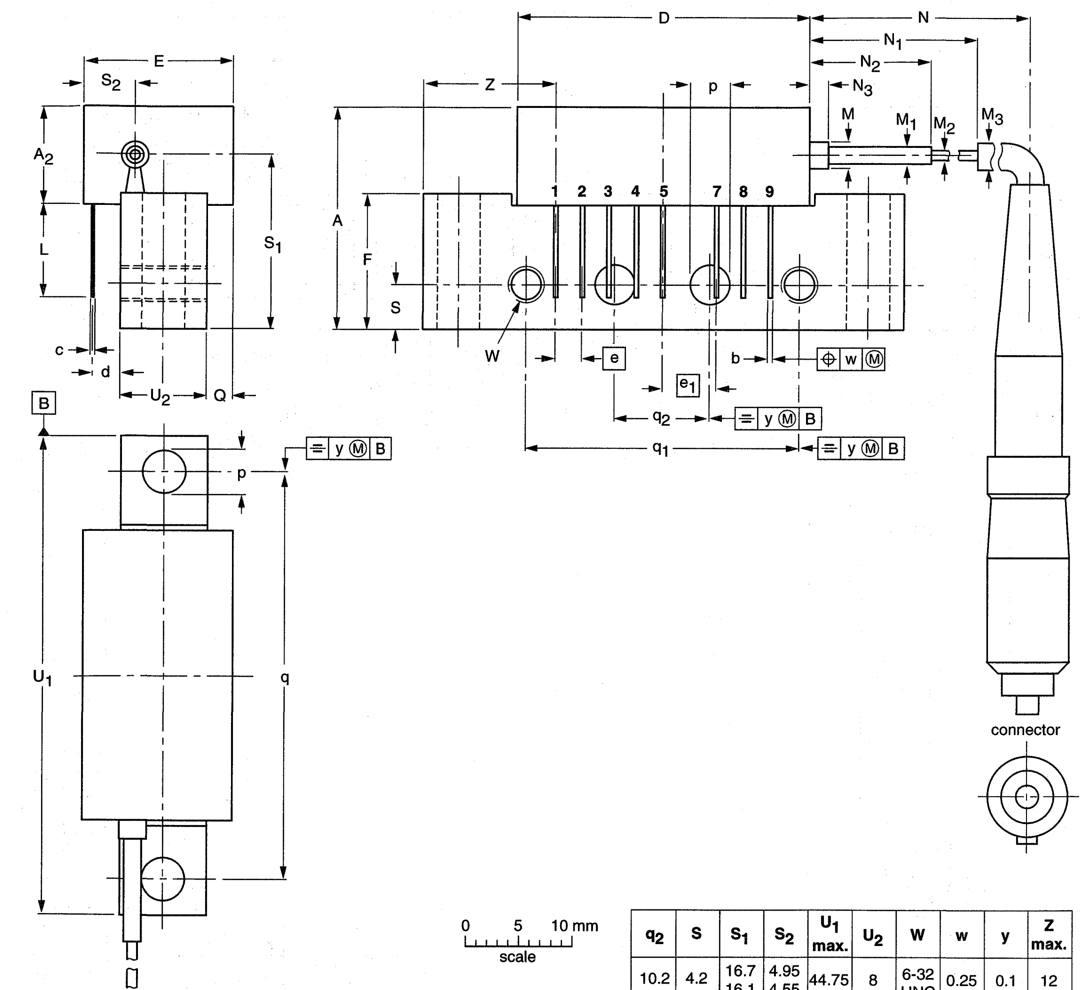
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	M	M_1	M_2	M_3	N	N_1	N_2	N_3	p	Q max.	q	q_1
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	917 817	15.3 8.7	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4

q_2	S	S_1	S_2	U_1 max.	U_2	W	w	y	Z max.
10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115V						99-02-06

Rectangular single-ended package; aluminium flange;
2 vertical mounting holes; 2 x 6-32 UNC and 2 extra horizontal mounting holes;
optical input with connector; 8 gold-plated in-line leads **SOT115W**



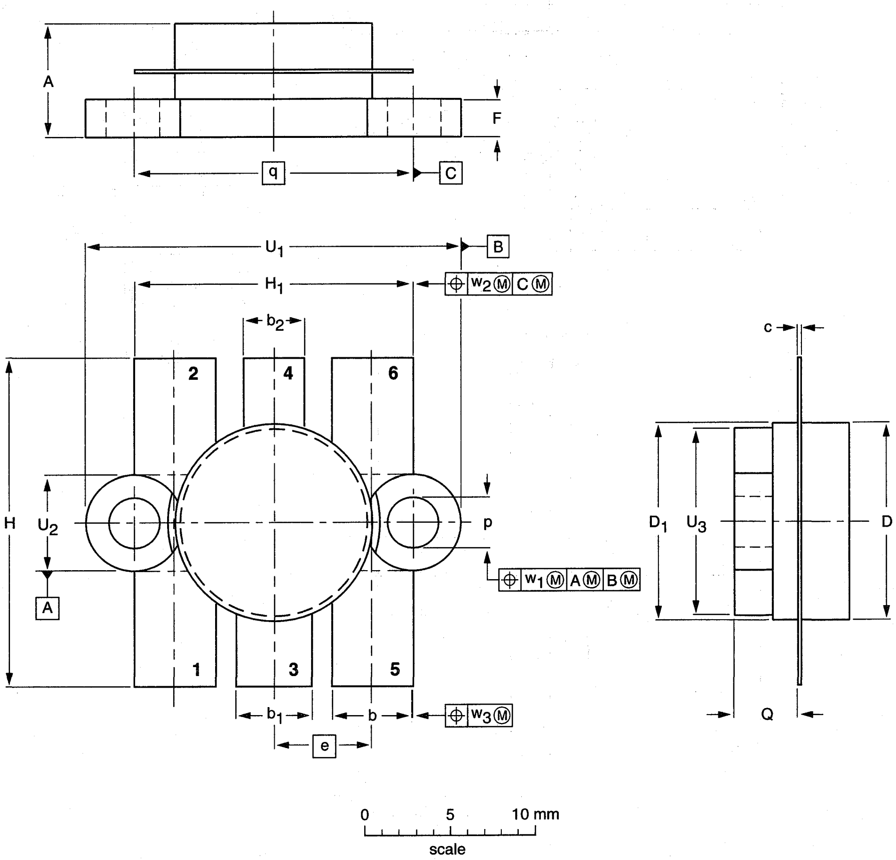
DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_2 max.	b	c	D max.	d max.	E max.	e	e_1	F	L min.	M	M_1	M_2	M_3	N	N_1	N_2	N_3	p	Q max.	q	q_1
mm	20.8	9.1	0.51 0.38	0.25	27.2	2.54	13.75	2.54	5.08	12.7	8.8	2.5	1.6	0.9	3	627 577	127 77	10.7 8.7	5 1	4.15 3.85	2.4	38.1	25.4

UNIT	q_2	S	S_1	S_2	U_1 max.	U_2	W	w	y	Z max.
mm	10.2	4.2	16.7 16.1	4.95 4.55	44.75	8	6-32 UNC	0.25	0.1	12

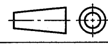
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT115W						99-04-13

Flanged ceramic package; 2 mounting holes; 6 leads **SOT119A**

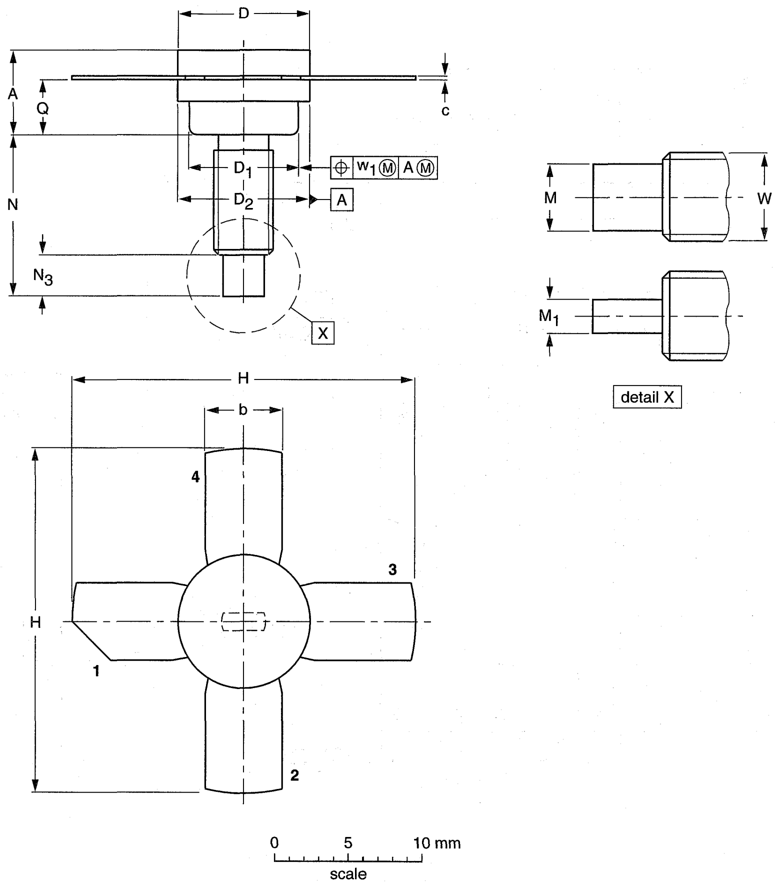


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	b_2	c	D	D_1	e	F	H	H_1	p	Q	q	U_1	U_2	U_3	w_1	w_2	w_3
mm	7.39 6.32	5.59 5.33	5.34 5.08	4.07 3.81	0.15 0.10	12.86 12.59	12.83 12.57	6.48	2.54 2.29	21.97 21.21	18.55 18.28	3.30 3.05	4.57 4.06	18.42	24.89 24.64	6.48 6.22	12.32 12.07	0.25	0.51	0.25
inches	0.291 0.249	0.220 0.210	0.210 0.200	0.160 0.150	0.006 0.004	0.505 0.496	0.505 0.495	0.255	0.100 0.090	0.865 0.835	0.730 0.720	0.130 0.120	0.180 0.160	0.725	0.980 0.970	0.255 0.245	0.485 0.475	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT119A						99-03-29

Studded ceramic package; 4 leads **SOT120A**

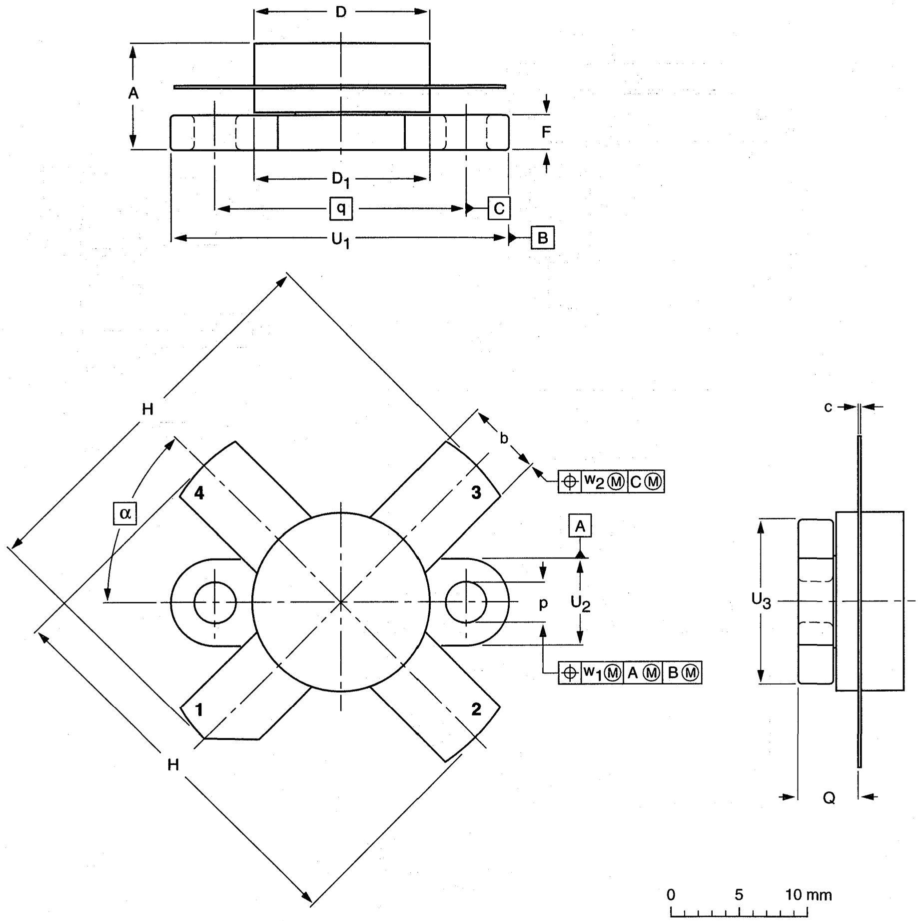


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	5.97 4.74	5.85 5.58	0.18 0.10	9.73 9.47	8.39 8.12	9.66 9.39	27.44 25.78	3.41 2.92	1.66 1.39	12.83 11.17	3.31 2.54	4.34 4.04	8-32 UNC	0.38
inches	0.283 0.248	0.230 0.220	0.006 0.004	0.383 0.373	0.330 0.320	0.380 0.370	1.080 1.015	0.134 0.115	0.065 0.055	0.505 0.440	0.130 0.100	0.171 0.159		0.015

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT120A						99-03-29

Flanged ceramic package; 2 mounting holes; 4 leads **SOT121B**

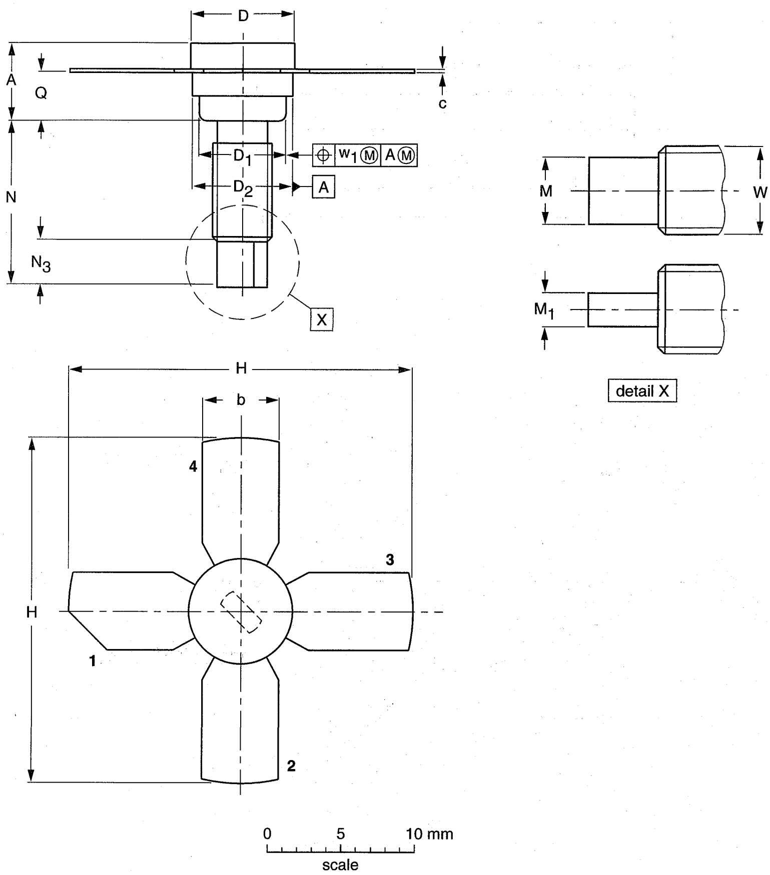


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.27 6.17	5.82 5.56	0.16 0.10	12.86 12.59	12.83 12.57	2.67 2.41	28.45 25.52	3.30 3.05	4.45 3.91	18.42	24.90 24.63	6.48 6.22	12.32 12.06	0.25	0.51	45°
inches	0.286 0.243	0.229 0.219	0.006 0.004	0.506 0.496	0.505 0.495	0.105 0.095	1.120 1.005	0.130 0.120	0.175 0.154	0.725	0.98 0.97	0.255 0.245	0.485 0.475	0.01	0.02	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT121B						99-03-29

Studded ceramic package; 4 leads **SOT122A**

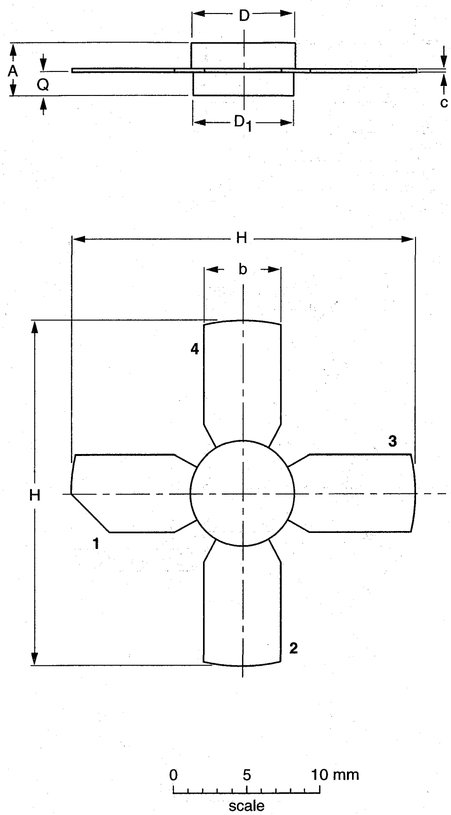


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	5.92 4.80	5.85 5.58	0.15 0.10	7.50 7.23	6.48 6.22	7.24 6.93	27.43 25.78	3.18 2.67	1.66 1.39	12.95 12.70	3.68 2.92	3.35 2.79	8-32 UNC	0.38
inches	0.233 0.189	0.230 0.220	0.006 0.004	0.295 0.285	0.255 0.245	0.285 0.273	1.080 1.015	0.125 0.105	0.065 0.055	0.510 0.500	0.145 0.115	0.132 0.110		0.015

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122A						99-03-29

Studless ceramic package; 4 leads **SOT122D**

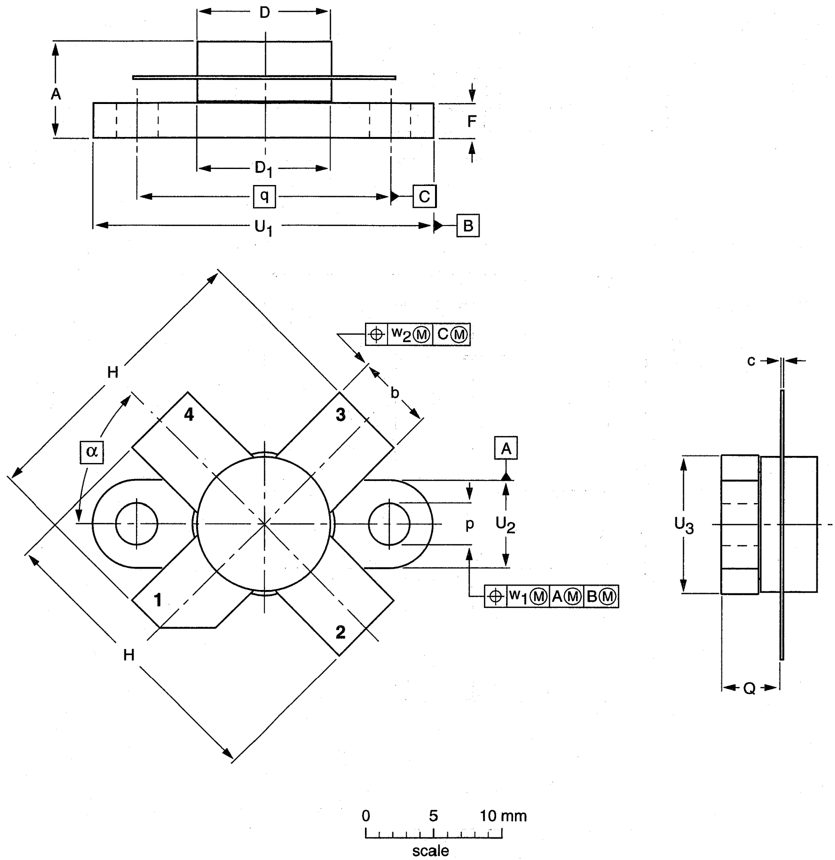


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	H	Q
mm	4.14 3.27	5.85 5.58	0.15 0.10	7.50 7.23	7.24 6.99	27.43 25.78	1.57 1.32
inches	0.163 0.129	0.230 0.220	0.006 0.004	0.295 0.285	0.285 0.275	1.080 1.015	0.062 0.052

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT122D						99-03-29

Flanged ceramic package; 2 mounting holes; 4 leads **SOT123A**

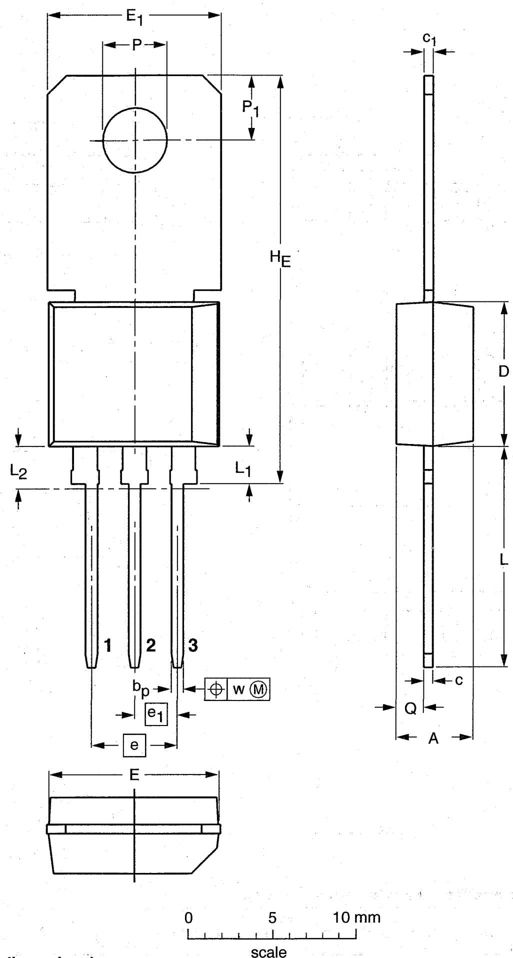


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	F	H	p	Q	q	U_1	U_2	U_3	w_1	w_2	α
mm	7.47 6.37	5.82 5.56	0.18 0.10	9.73 9.47	9.78 9.42	2.72 2.31	20.71 19.93	3.33 3.04	4.63 4.11	18.42	24.87 24.64	6.48 6.22	9.78 9.39	0.25	0.51	45°
inches	0.294 0.251	0.229 0.219	0.007 0.004	0.383 0.373	0.385 0.371	0.107 0.091	0.815 0.785	0.131 0.120	0.182 0.162	0.725	0.980 0.970	0.255 0.245	0.385 0.370	0.010	0.020	

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT123A						99-03-29

Plastic single-ended leaded (through hole) package; with cooling fin, mountable to heatsink, 1 mounting hole; 3 leads (in-line) **SOT128B**



DIMENSIONS (mm are the original dimensions)

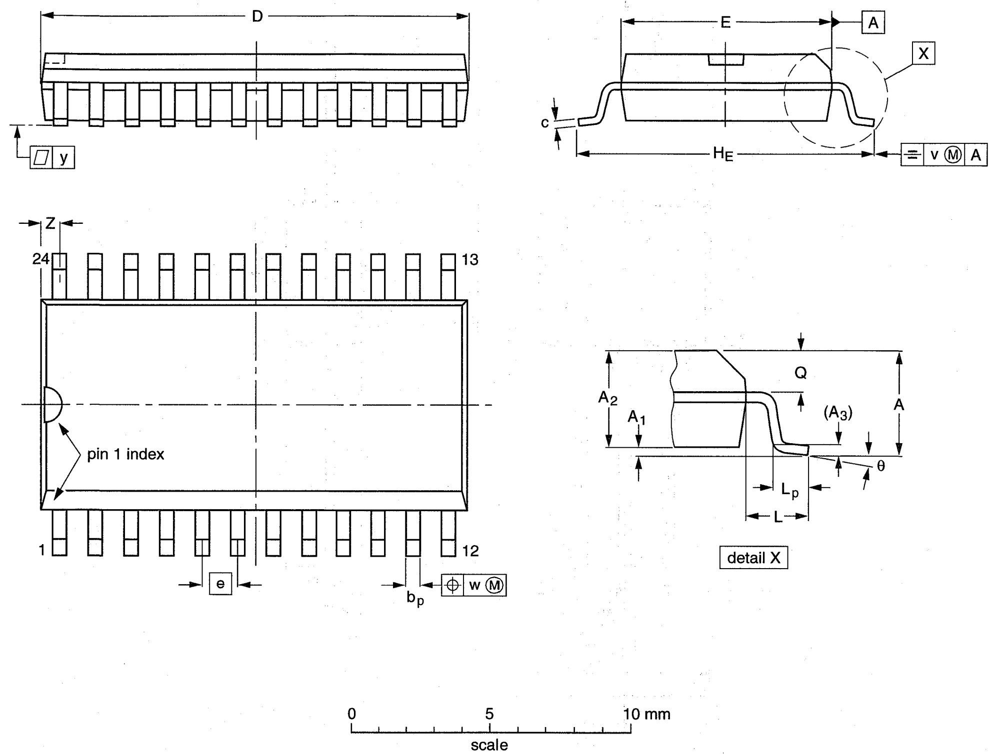
UNIT	A	b_p	c	c_1	D	E	E_1	e	e_1	H_E	L	L_1	$L_2^{(1)}$ max	P	P_1	Q	w
mm	4.6 4.4	0.8 0.6	0.65 0.5	0.56 0.46	8.6 8.4	10.1 9.9	10.4 10.0	5.08	2.54	24.2 23.8	13.3 12.2	2.4 2.0	2.5	3.8 3.6	3.9 3.7	1.7 1.5	0.25

Note

1. Plastic flash allowed within this zone

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT128B		TO-202				97-02-28

SO24: plastic small outline package; 24 leads; body width 7.5 mm **SOT137-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

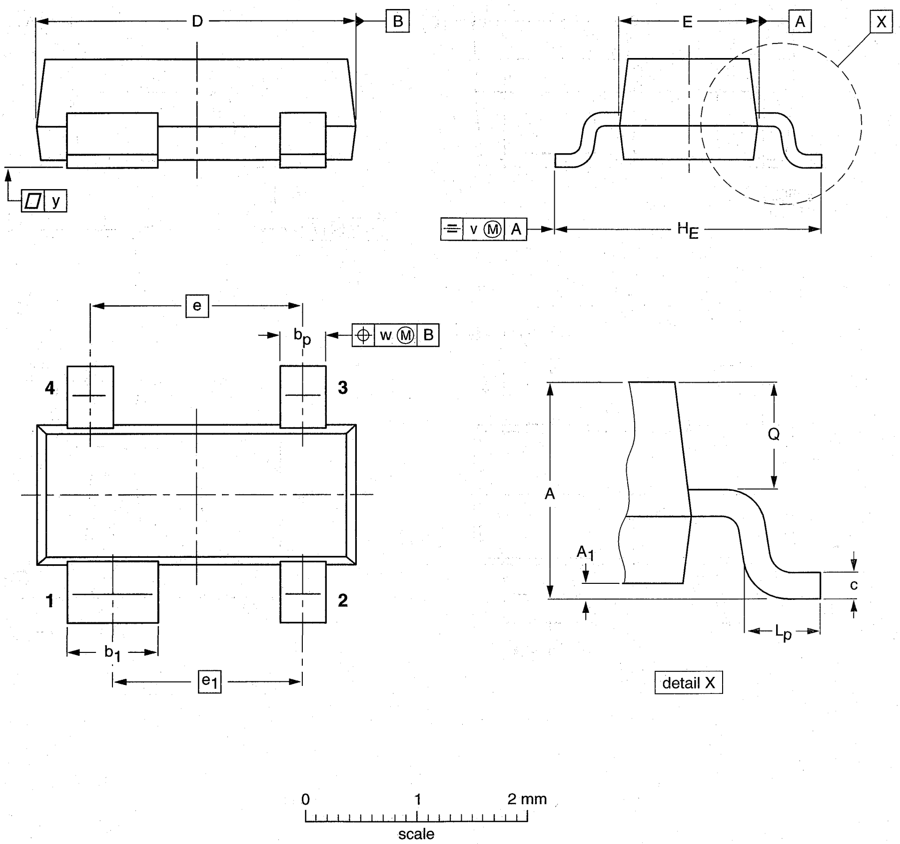
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	15.6 15.2	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.61 0.60	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT137-1	075E05	MS-013AD				~~95-01-24~~ 97-05-22

Plastic surface mounted package; 4 leads **SOT143B**



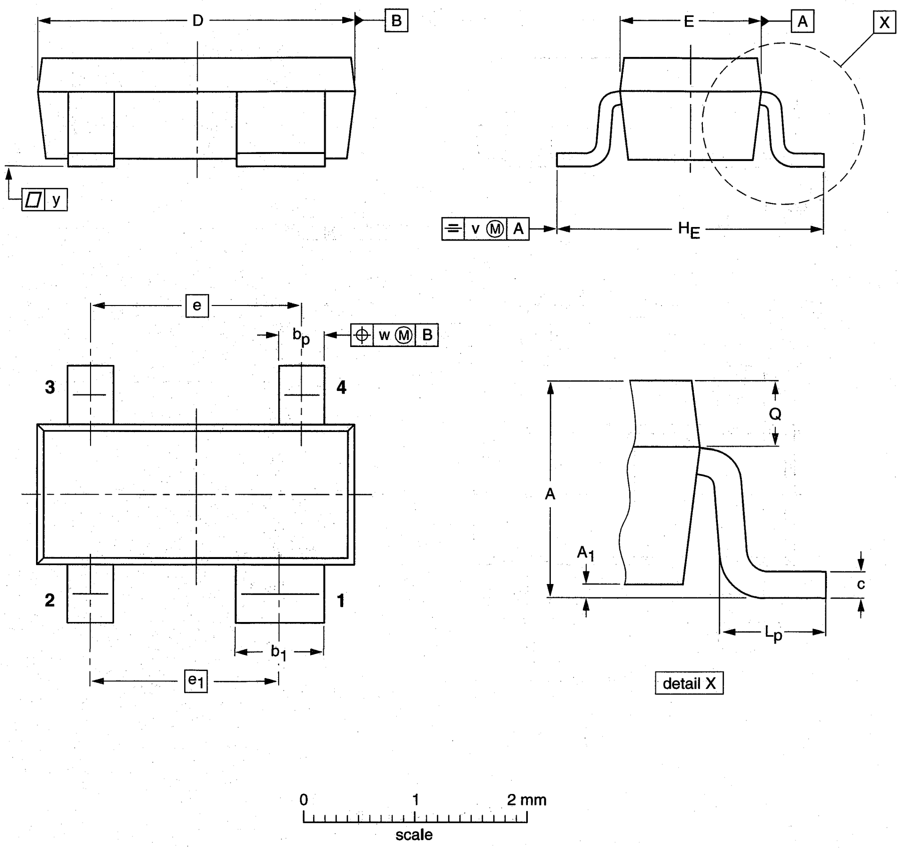
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.45 0.15	0.55 0.45	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143B						97-02-28

Package outlines Chapter 2

Plastic surface mounted package; reverse pinning; 4 leads **SOT143R**

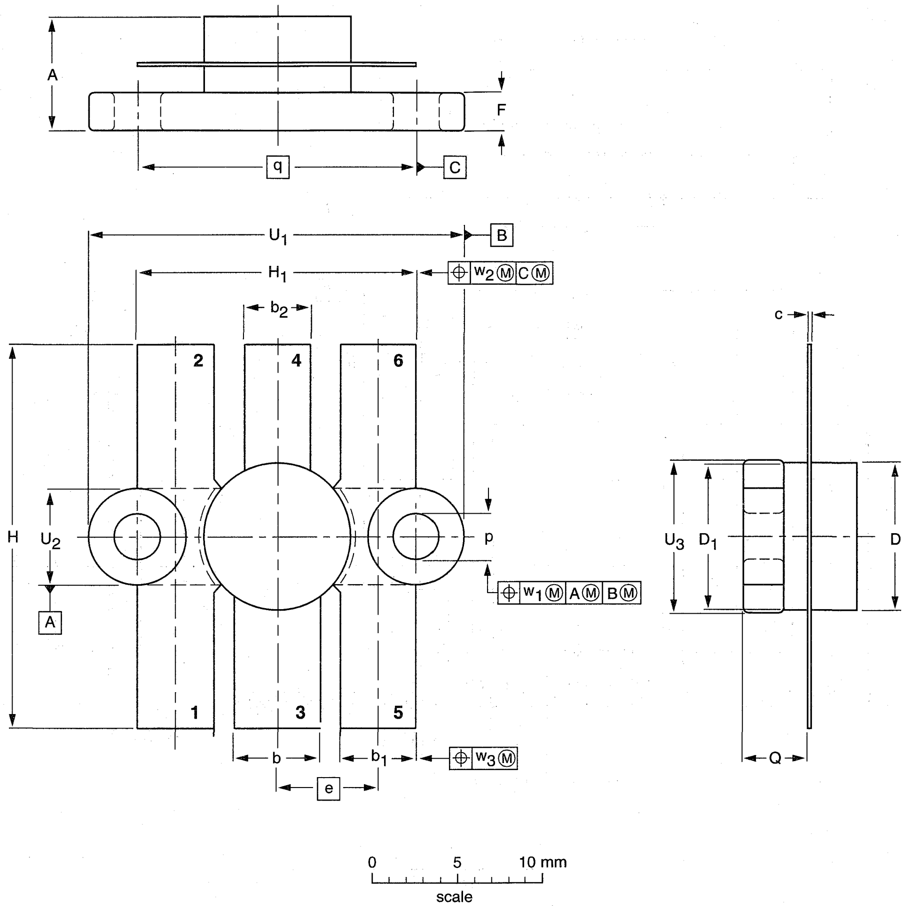


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.48 0.38	0.88 0.78	0.15 0.09	3.0 2.8	1.4 1.2	1.9	1.7	2.5 2.1	0.55 0.25	0.45 0.25	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT143R						97-03-10

Flanged ceramic package; 2 mounting holes; 6 leads **SOT160A**

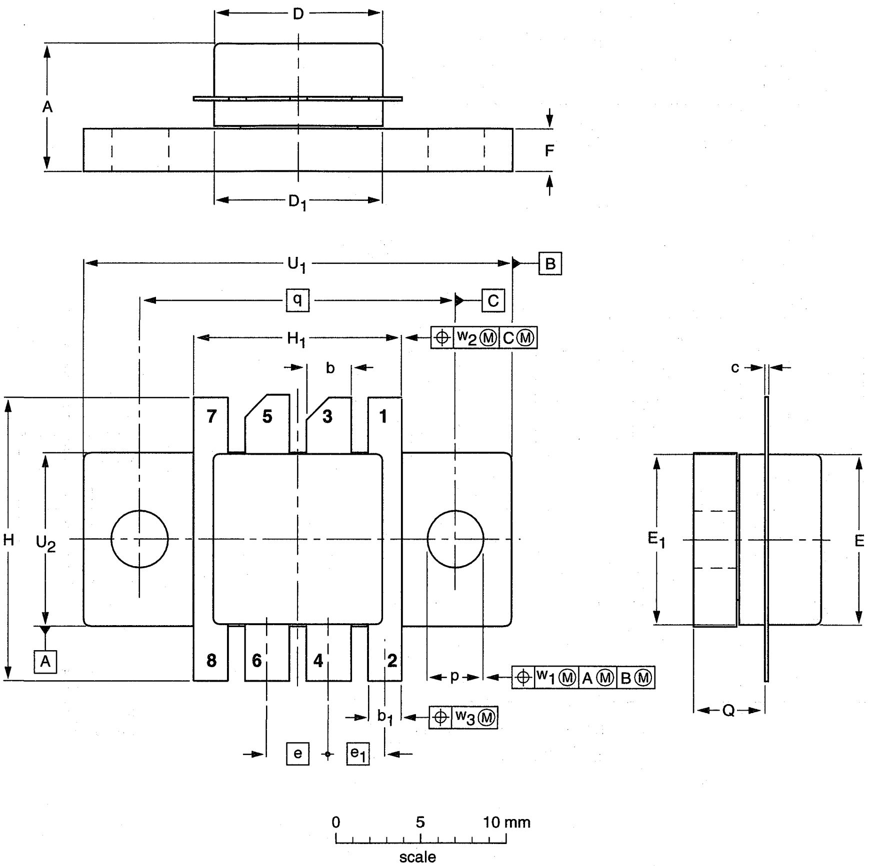


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	b_2	c	D	D_1	e	F	H	H_1	p	Q	q	U_1	U_2	U_3	w_1	w_2	w_3
mm	7.32 6.40	5.72 5.46	5.21 4.95	4.70 4.44	0.16 0.10	9.73 9.47	9.66 9.39	6.60	2.85 2.23	24.39 23.87	18.42 18.16	3.31 3.04	4.50 4.14	18.42	24.90 24.63	6.48 6.22	9.78 9.52	0.25	0.51	0.25
inches	0.288 0.252	0.225 0.215	0.205 0.195	0.185 0.175	0.004 0.006	0.383 0.373	0.380 0.370	0.260	0.112 0.088	0.960 0.940	0.725 0.715	0.130 0.120	0.177 0.163	0.725	0.980 0.970	0.255 0.245	0.385 0.375	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT160A						99-03-29

Flanged ceramic package; 2 mounting holes; 8 leads **SOT161A**

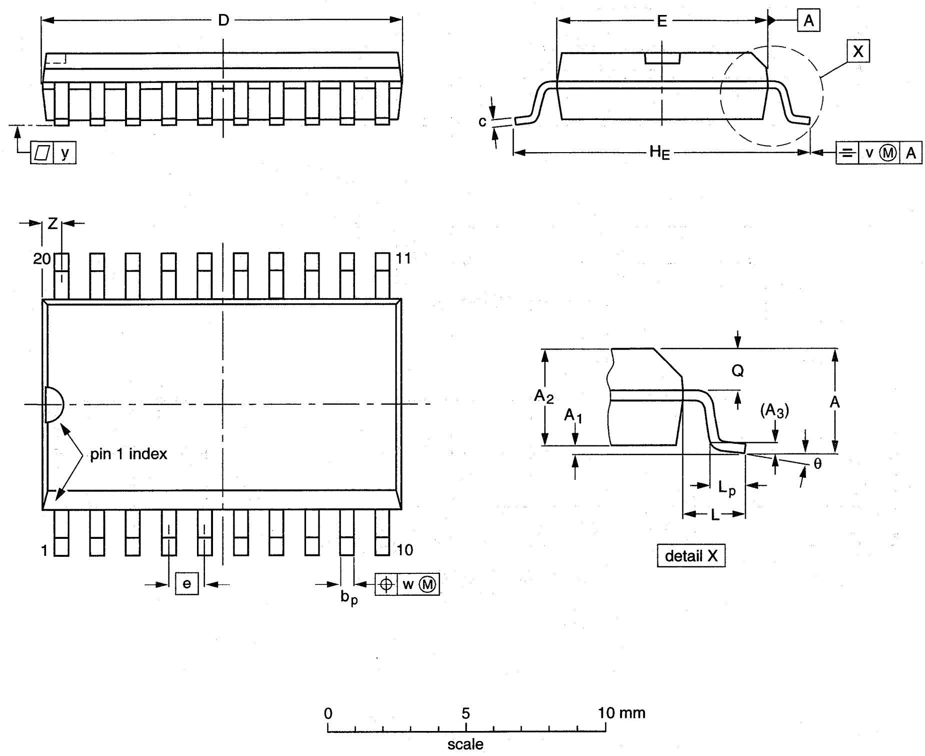


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	e_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.27 6.47	2.93 2.66	2.04 1.77	0.18 0.10	10.22 10.00	10.21 9.94	10.21 10.00	10.21 9.94	3.80	3.50	2.70 2.08	16.81 16.21	12.83 12.57	3.33 3.07	4.32 4.06	18.42	24.97 24.71	10.34 10.08	0.25	0.51	0.25
inches	0.286 0.255	0.115 0.105	0.080 0.070	0.007 0.004	0.402 0.394	0.402 0.391	0.402 0.394	0.402 0.391	0.150	0.138	0.106 0.082	0.662 0.638	0.505 0.495	0.131 0.121	0.170 0.160	0.725	0.983 0.973	0.407 0.397	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT161A						99-03-29

SO20: plastic small outline package; 20 leads; body width 7.5 mm **SOT163-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

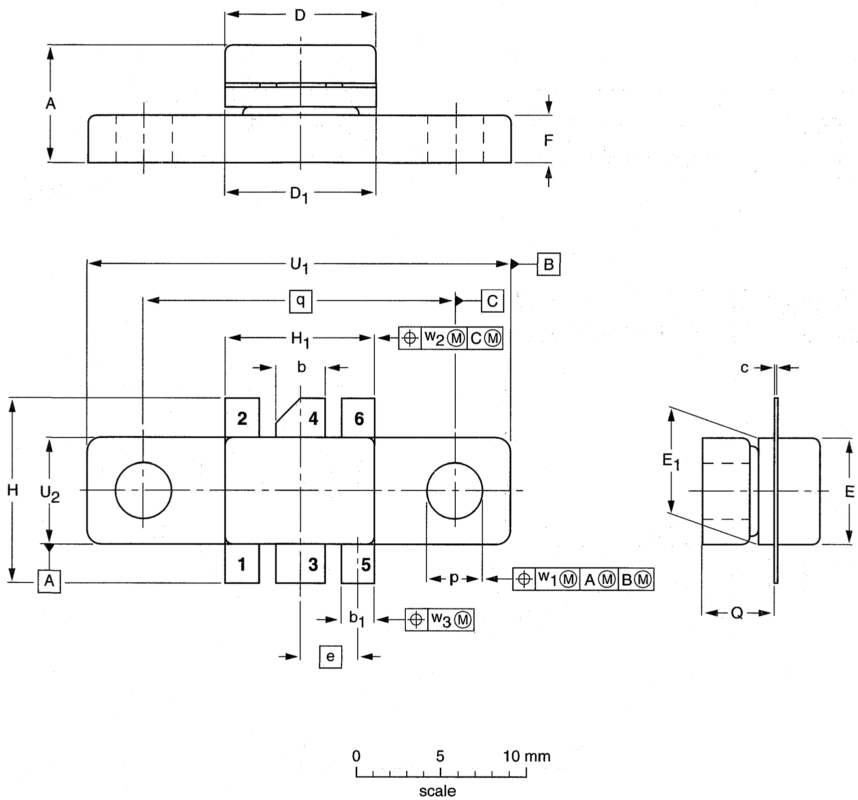
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.419 0.394	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

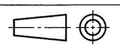
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				~~95-01-24~~ 97-05-22

Flanged ceramic package; 2 mounting holes; 6 leads **SOT171A**

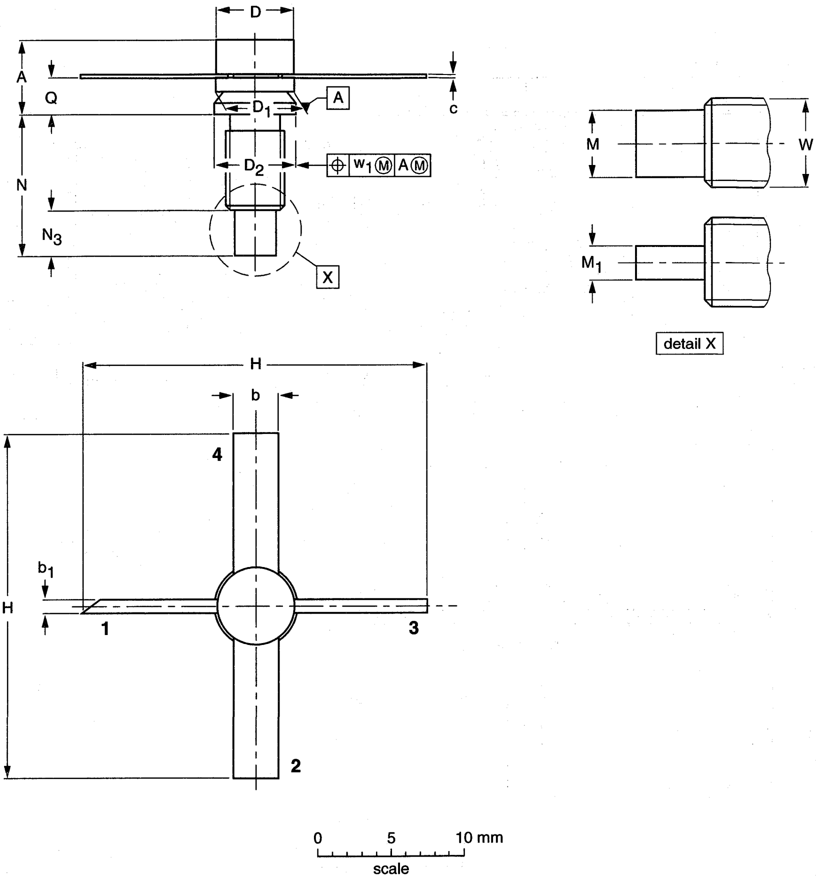


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.81 6.07	3.18 2.92	2.13 1.88	0.16 0.07	9.25 9.04	9.27 9.02	5.95 5.74	5.97 5.72	3.58	3.05 2.54	11.31 10.54	9.27 9.01	3.43 3.17	4.32 4.11	18.42	24.90 24.63	5.97 5.72	0.25	0.51	0.25
inches	0.268 0.239	0.125 0.115	0.084 0.074	0.006 0.003	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.140	0.120 0.100	0.445 0.415	0.365 0.355	0.135 0.125	0.170 0.162	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT171A						99-03-29

Studded ceramic package; 4 leads **SOT172A1**

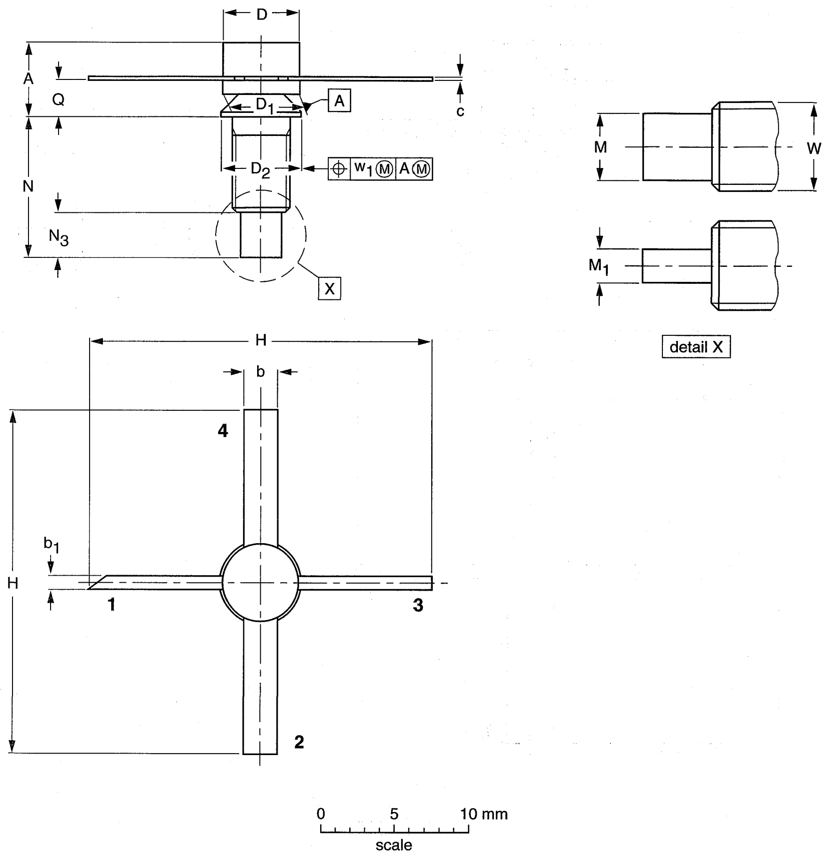


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	5.31 4.34	3.31 3.04	0.89 0.63	0.16 0.10	5.20 4.95	5.33 5.08	5.33 5.08	26.17 24.63	3.05 2.79	1.66 1.39	11.82 10.89	3.69 2.92	2.74 2.34	8-32 UNC	0.38
inches	0.209 0.171	0.130 0.120	0.035 0.025	0.006 0.004	0.205 0.195	0.210 0.200	0.210 0.200	1.030 0.970	0.120 0.110	0.065 0.055	0.465 0.429	0.145 0.115	0.108 0.092		0.015

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172A1						99-03-29

Studded ceramic package; 4 leads **SOT172A2**

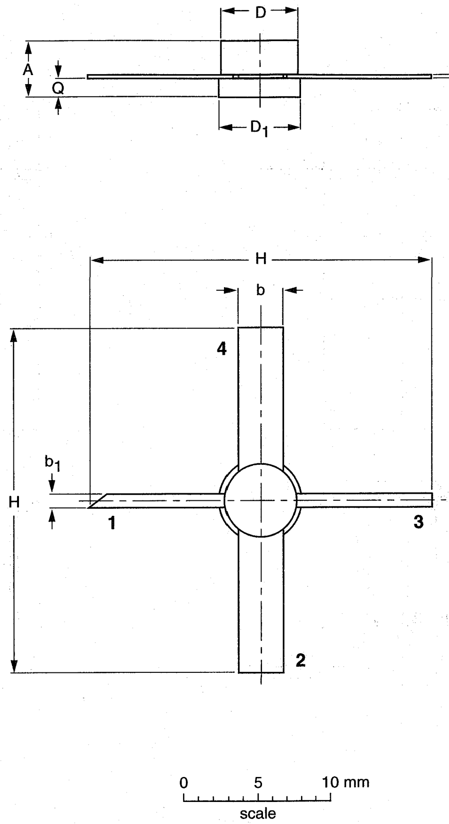


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	5.51 4.45	1.66 1.39	0.89 0.63	0.16 0.10	5.20 4.95	5.31 5.05	5.33 5.08	23.37 22.35	3.05 2.79	1.66 1.39	11.56 11.05	3.43 3.18	2.95 2.43	8-32 UNC	0.38
inches	0.217 0.175	0.065 0.055	0.035 0.025	0.006 0.004	0.205 0.195	0.209 0.199	0.210 0.200	0.920 0.880	0.120 0.110	0.065 0.055	0.455 0.435	0.135 0.125	0.116 0.096		0.015

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172A2						99-03-29

Studless ceramic package; 4 leads **SOT172D**

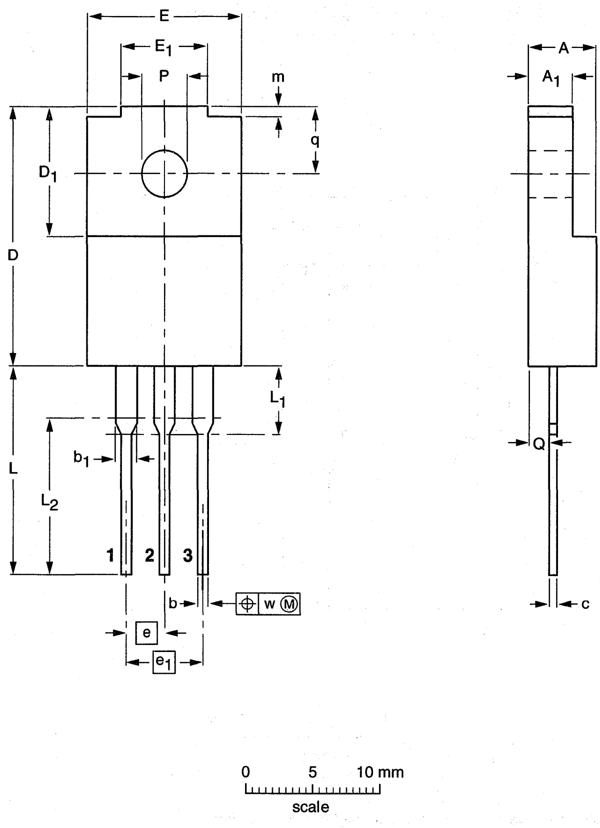


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	H	Q
mm	3.71 2.89	3.31 3.04	0.89 0.63	0.16 0.10	5.20 4.95	5.33 5.08	26.17 24.63	1.15 0.88
inches	0.146 0.114	0.13 0.12	0.035 0.025	0.006 0.004	0.205 0.195	0.210 0.200	1.03 0.97	0.045 0.035

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT172D						97-06-28

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 exposed tabs **SOT186**



DIMENSIONS (mm are the original dimensions)

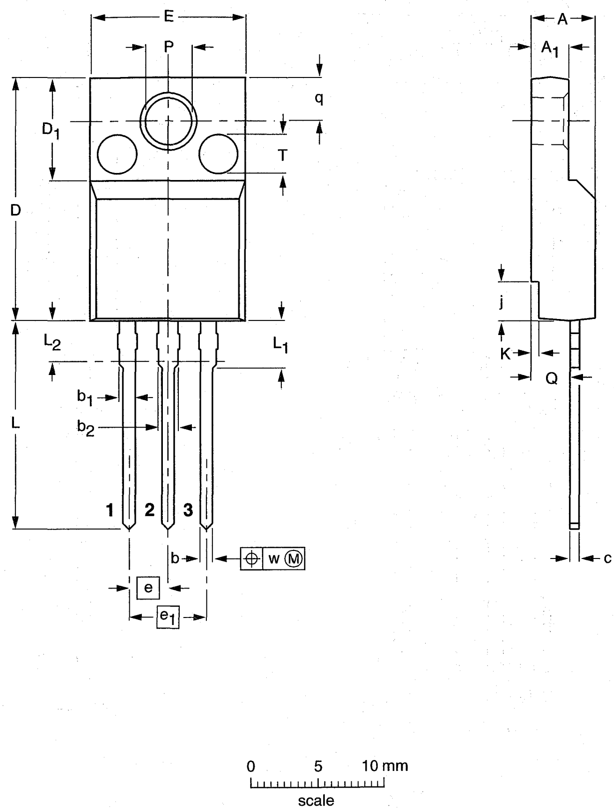
UNIT	A	A_1	b	b_1	c	D	D_1	E	E_1	e	e_1	L	L_1(1)	L_2	m	P	Q	q	w
mm	4.4 4.0	2.9 2.5	0.9 0.7	1.5 1.3	0.55 0.38	17.0 16.4	7.9 7.5	10.2 9.6	5.7 5.3	2.54	5.08	14.3 13.5	4.8 4.0	10	0.9 0.5	3.2 3.0	1.4 1.2	4.4 4.0	0.4

Note

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186		TO-220				97-06-11

Plastic single-ended package; isolated heatsink mounted; 1 mounting hole; 3 lead TO-220 **SOT186A**



DIMENSIONS (mm are the original dimensions)

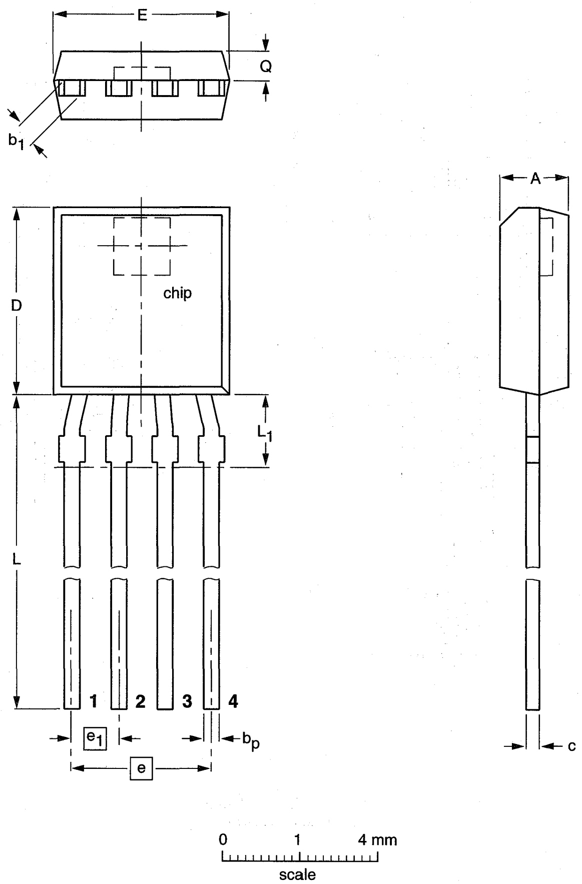
UNIT	A	A_1	b	b_1	b_2	c	D	D_1	E	e	e_1	j	K	L	L_1	L_2 (1) max.	P	Q	q	T (2)	w
mm	4.6 4.0	2.9 2.5	0.9 0.7	1.1 0.9	1.4 1.2	0.7 0.4	15.8 15.2	6.5 6.3	10.3 9.7	2.54	5.08	2.7 2.3	0.6 0.4	14.4 13.5	3.30 2.79	3	3.2 3.0	2.6 2.3	3.0 2.6	2.5	0.4

Notes

1. Terminal dimensions within this zone are uncontrolled. Terminals in this zone are not tinned.
2. Both recesses are ∅ 2.5 × 0.8 max. depth

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT186A		TO-220				97-06-11

Plastic single-ended flat package; 4 in-line leads **SOT195**



DIMENSIONS (mm are the original dimensions)

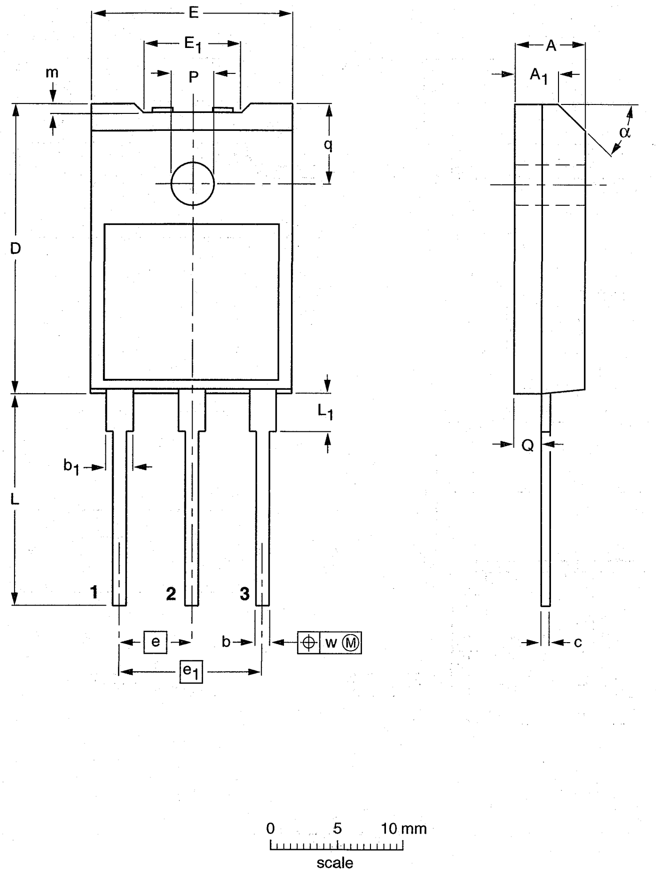
UNIT	A	b_p	b_1	c	D	E	e	e_1	L	L_1 (1) max.	Q
mm	1.8 1.6	0.48 0.40	0.7 0.5	0.45 0.39	5.2 5.0	4.8 4.4	3.75	1.25	14.5 12.7	2	0.8 0.7

Notes

1. Terminal dimensions within this zone are uncontrolled to allow for flow of plastic and terminal irregularities.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT195						97-06-02

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3 leads (in-line) **SOT199**



DIMENSIONS (mm are the original dimensions)

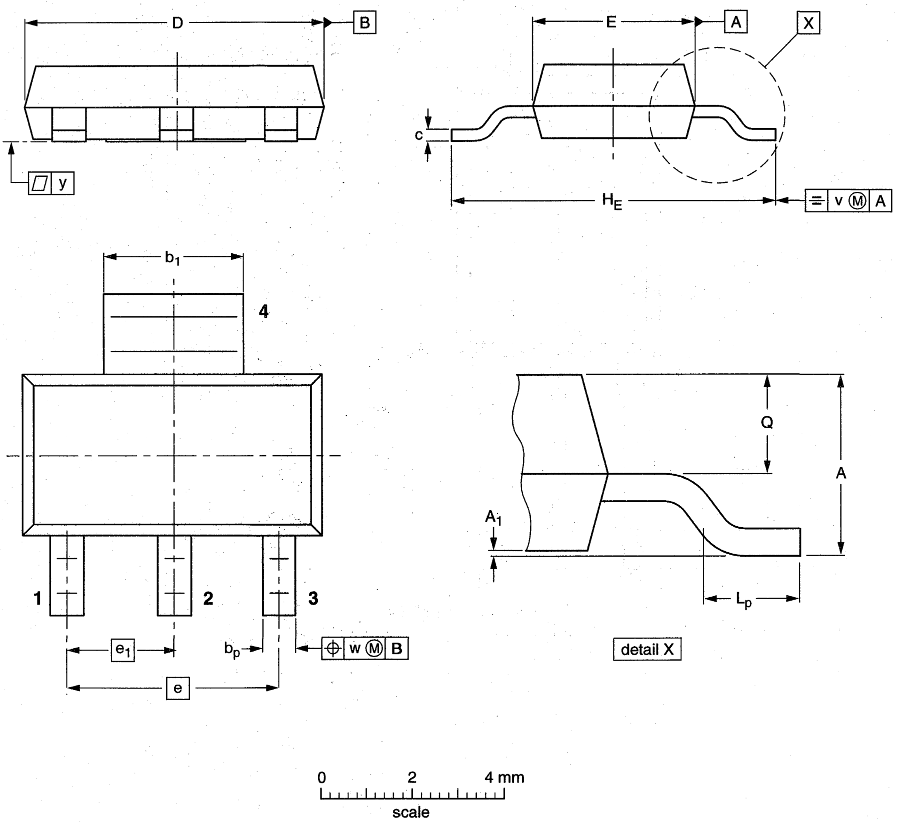
UNIT	A	A_1	b	b_1	c	D	E	E_1	e	e_1	L	L_1(1)	m	P	Q	q	w	α
mm	5.2 4.8	3.4 3.0	1.2 1.0	2.1 1.9	0.6 0.5	21.5 20.5	15.3 14.7	7.8 6.8	5.45	10.9	16.5 15.7	3.7 3.3	0.8 0.6	3.3 3.1	2.1 1.9	6.2 5.8	0.4	45°

Note

1. Terminals in this zone are not tinned.

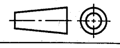
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT199						97-06-27

Plastic surface mounted package; collector pad for good heat transfer; 4 leads **SOT223**



DIMENSIONS (mm are the original dimensions)

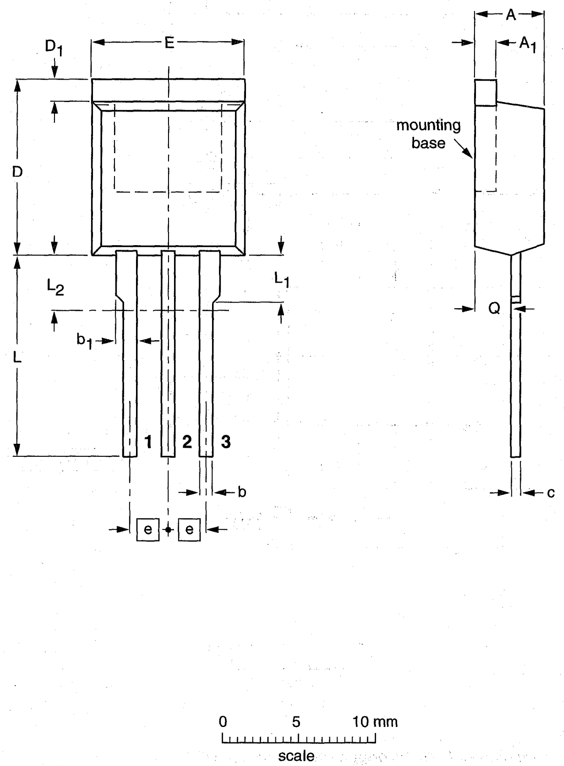
UNIT	A	A_1	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.8 1.5	0.10 0.01	0.80 0.60	3.1 2.9	0.32 0.22	6.7 6.3	3.7 3.3	4.6	2.3	7.3 6.7	1.1 0.7	0.95 0.85	0.2	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT223						~~96-11-11~~ 97-02-28

Package outlines

Chapter 2

Plastic single-ended package; 3 lead low-profile TO-220 **SOT226**



DIMENSIONS (mm are the original dimensions)

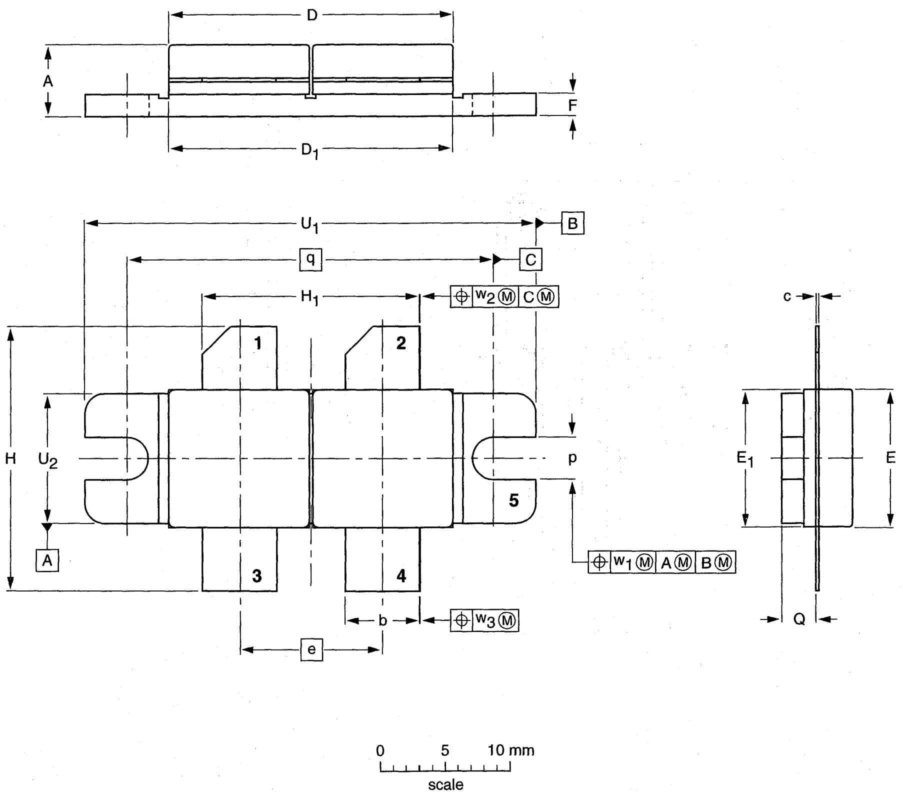
UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1	L_2[(1)] max	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	2.6 2.2

Note

1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT226		low-profile TO-220				97-06-11

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A1**

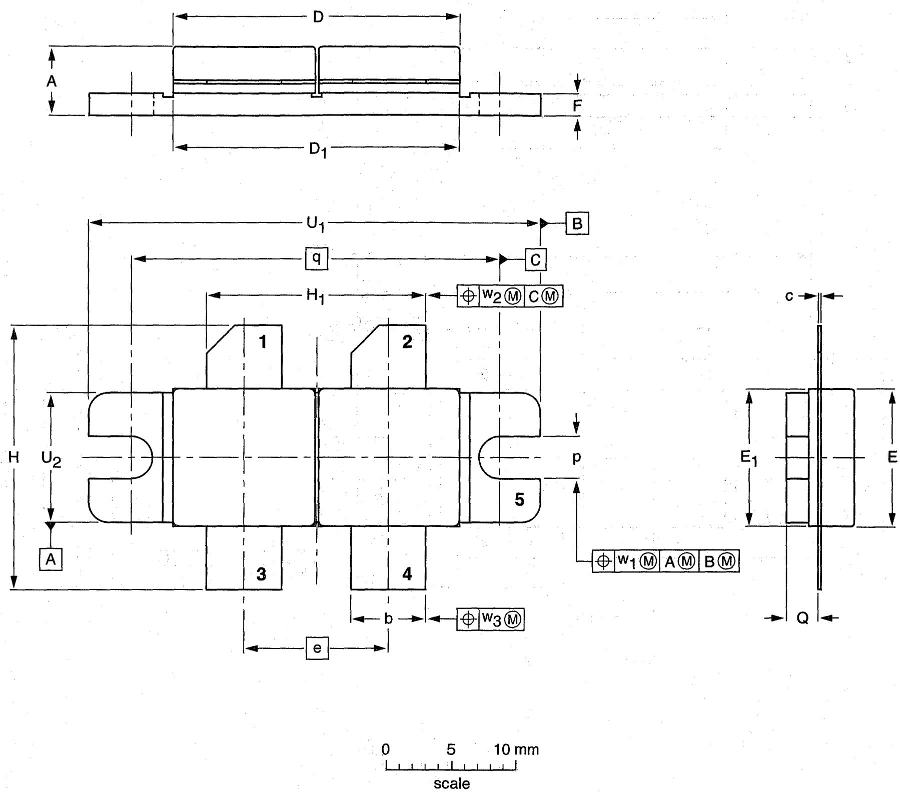


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.85 2.59	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.112 0.102	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A1						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT262A2**

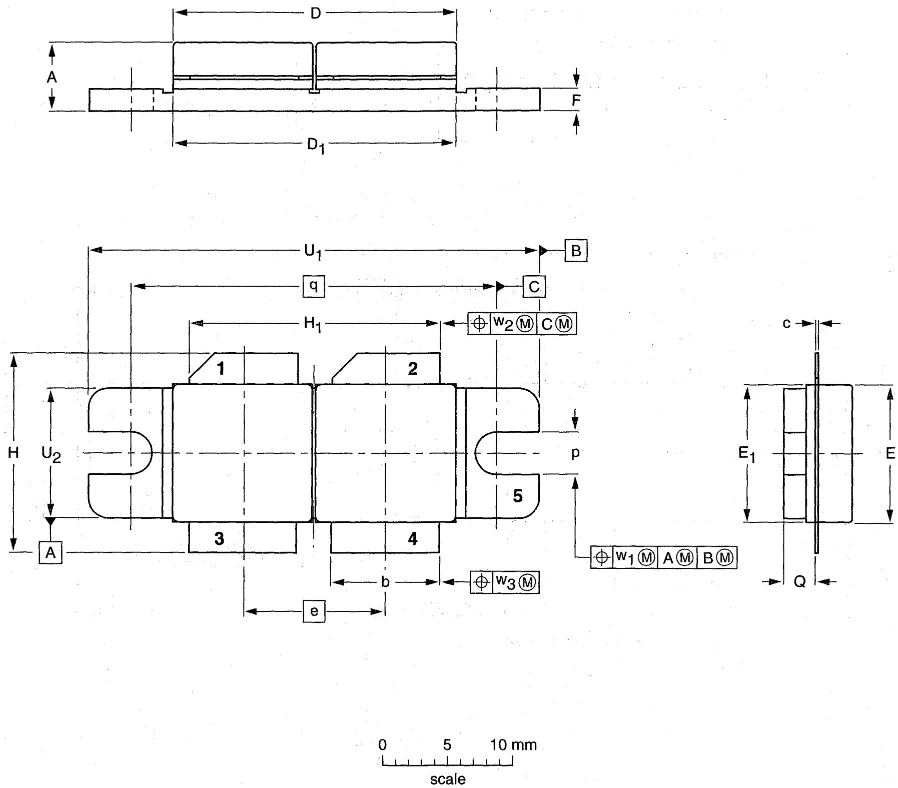


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	5.85 5.58	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	21.08 19.56	17.02 16.51	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.230 0.220	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.830 0.770	0.670 0.650	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262A2						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads — SOT262B

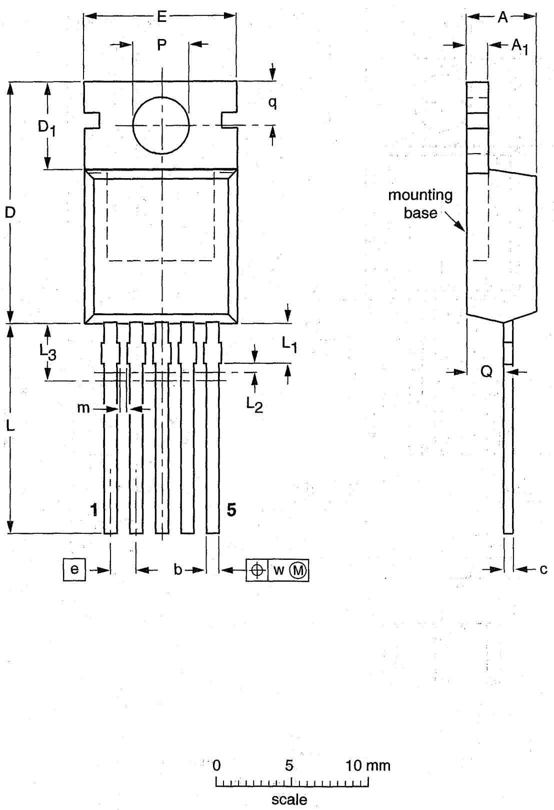


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.39 4.62	8.51 8.25	0.16 0.10	22.17 21.46	21.98 21.71	11.05	10.27 10.05	10.29 10.03	1.78 1.52	15.49 14.99	19.69 19.17	3.28 3.02	2.47 2.20	27.94	34.17 33.90	9.91 9.65	0.25	0.51	0.25
inches	0.212 0.182	0.335 0.325	0.006 0.004	0.873 0.845	0.865 0.855	0.435	0.404 0.396	0.405 0.396	0.070 0.060	0.61 0.59	0.775 0.755	0.129 0.119	0.097 0.087	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT262B						99-03-29

Plastic single-ended package; heatsink mounted; 1 moumting hole; 5-lead TO-220 — SOT263



DIMENSIONS (mm are the original dimensions)

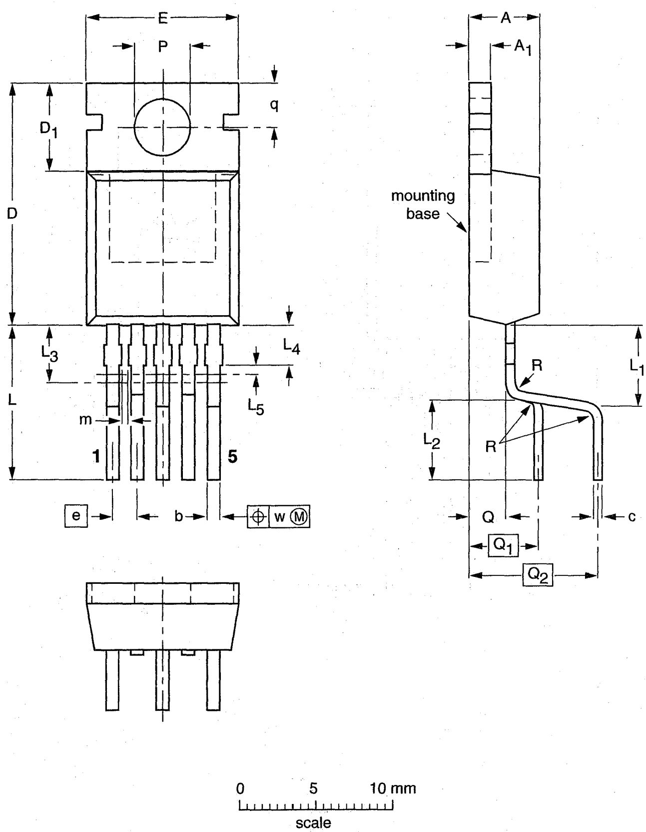
UNIT	A	A_1	b	c	D	D_1	E	e	L	L_1 (1)	L_2 (2)	L_3 (3) max.	m	P	q	Q	w
mm	4.5 4.1	1.39 1.27	0.9 0.7	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	1.7	15.0 13.5	2.4 1.6	0.5	3.5	0.8 0.6	3.8 3.6	3.0 2.7	2.6 2.2	0.4

Notes

1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT263		5-lead TO-220				97-06-11

Plastic single-ended package; heatsink mounted; 1 mounting hole; 5-lead TO-220 lead form option **SOT263-01**



DIMENSIONS (mm are the original dimensions)

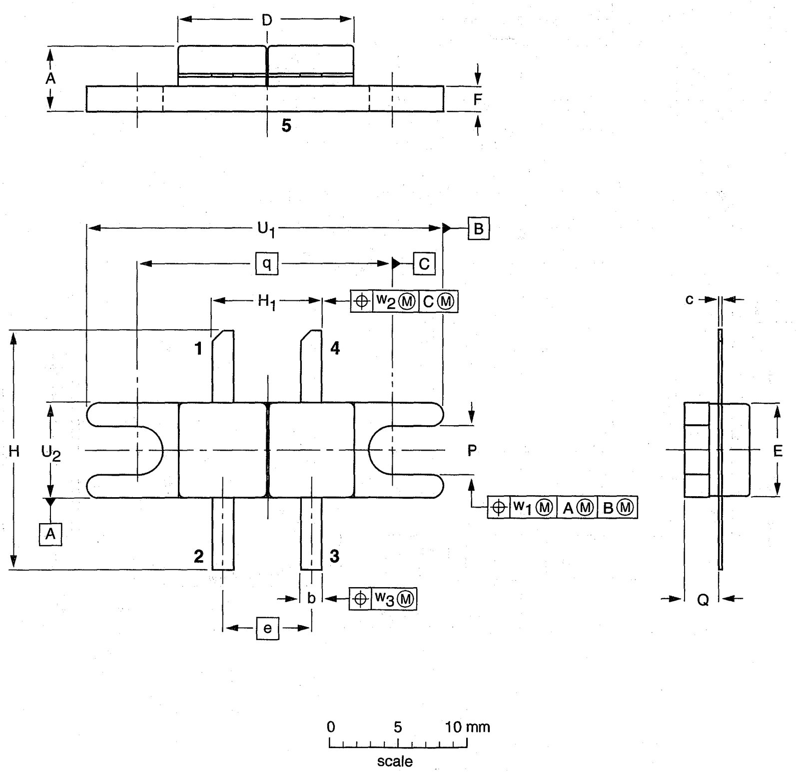
UNIT	A	A1	b	c	D	D1	E	e	L	L1	L2	L3(1) max.	L4(2)	L5(3) max.	m	P	q	Q	Q1	Q2	R	w
mm	4.5 4.1	1.39 1.27	0.90 0.75	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	1.7	9.8 9.7	5.9 5.3	5.2 5.0	3.5	2.4 1.6	0.5	0.8 0.6	3.8 3.6	3.0 2.7	2.0	4.5	8.2	0.5	0.4

Notes

1. Terminals in this zone are not tinned.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminal dimensions are uncontrolled in this zone.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT263-01		5-lead (option) TO-220				97-06-11

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT268A**

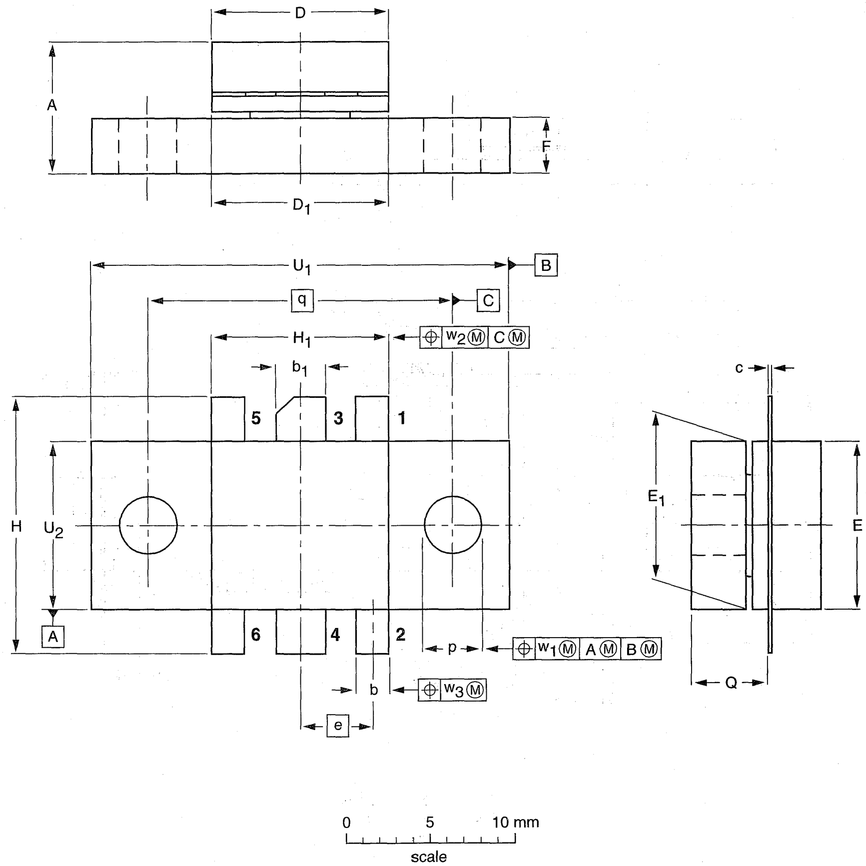


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.91 4.19	1.66 1.39	0.13 0.07	12.96 12.44	6.48 6.22	6.45	2.04 1.77	17.02 16.00	8.23 7.72	3.43 3.17	2.67 2.41	18.42	24.90 24.63	6.61 6.35	0.25	0.51	0.25
inches	0.193 0.165	0.065 0.055	0.005 0.003	0.510 0.490	0.255 0.245	0.254	0.080 0.070	0.670 0.630	0.324 0.304	0.135 0.125	0.105 0.095	0.725	0.980 0.970	0.260 0.250	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT268A						99-03-29

Flanged ceramic package; 2 mounting holes; 6 leads **SOT273A**

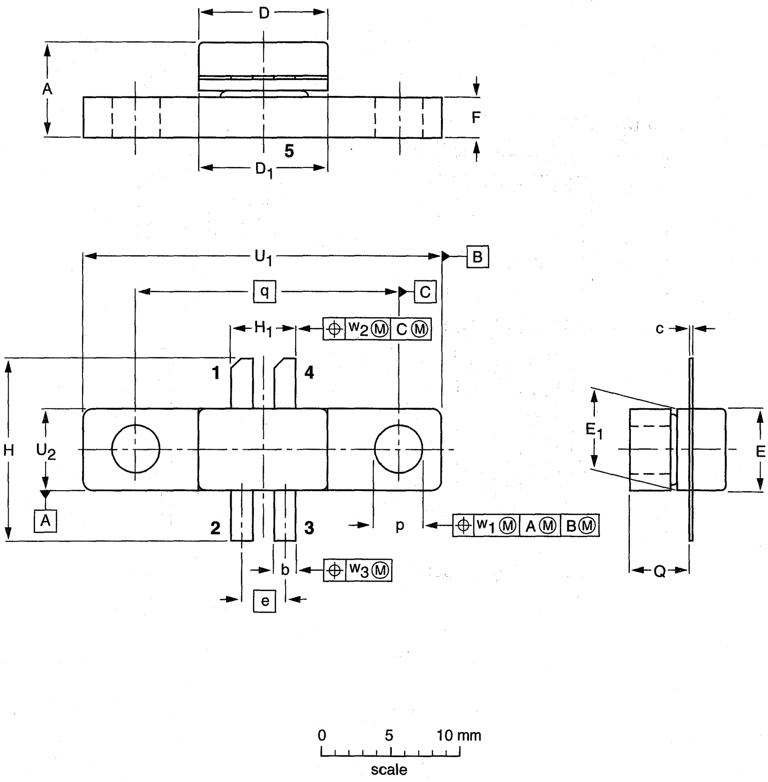


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	7.26 6.45	2.23 1.98	3.16 2.92	0.15 0.10	10.87 10.67	10.92 10.67	10.26 10.06	10.29 10.03	4.35	3.30 3.05	15.75 14.73	10.92 10.67	3.30 3.05	4.34 4.04	18.42	24.89 24.64	10.29 10.03	0.25	0.51	0.25
inches	0.286 0.254	0.088 0.078	0.125 0.115	0.006 0.004	0.428 0.420	0.430 0.420	0.404 0.396	0.405 0.395	0.171	0.130 0.120	0.620 0.580	0.430 0.420	0.130 0.120	0.171 0.159	0.725	0.980 0.970	0.405 0.395	0.010	0.020	0.010

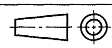
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT273A						99-03-29

Flanged double-ended ceramic package; 2 mounting holes; 4 leads **SOT279A**

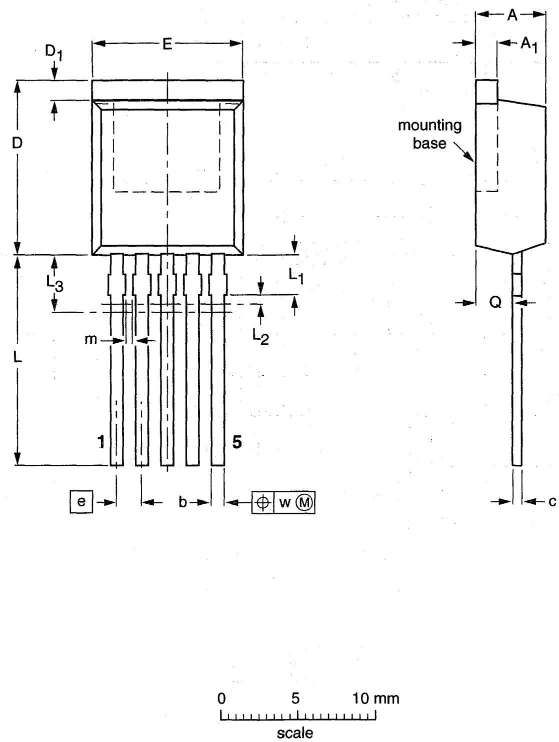


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	6.84 6.01	1.65 1.40	0.15 0.10	9.25 9.04	9.27 9.02	5.94 5.74	5.97 5.72	3.05	3.05 2.54	12.96 11.94	4.96 4.19	3.48 3.23	4.34 4.04	18.42	24.90 24.64	5.97 5.72	0.25	0.51	0.25
inches	0.269 0.237	0.065 0.055	0.006 0.004	0.364 0.356	0.365 0.355	0.234 0.226	0.235 0.225	0.120	0.120 0.100	0.510 0.470	0.195 0.165	0.137 0.127	0.171 0.159	0.725	0.980 0.970	0.235 0.225	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT279A						99-03-29

Plastic single-ended package; 5-lead low-profile TO-220 **SOT281**

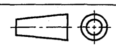


DIMENSIONS (mm are the original dimensions)

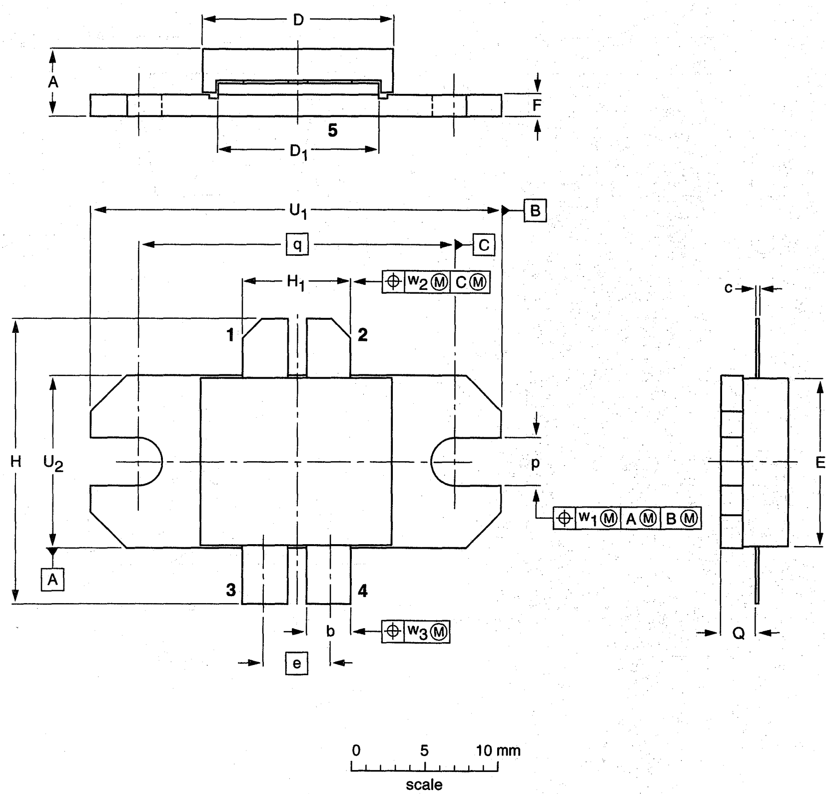
UNIT	A	A_1	b	c	D	D_1	E	e	L	L_1 (1)	L_2 (2)	L_3 (3) max.	m	Q	w
mm	4.5 4.1	1.39 1.27	0.9 0.7	0.7 0.4	11.0 10.0	1.5 1.1	10.3 9.7	1.7	15.0 13.5	2.4 1.6	0.5	3.5	0.8 0.6	2.6 2.2	0.4

Notes

1. Terminal dimensions are uncontrolled in this zone.
2. Positional accuracy of the terminals is controlled in this zone.
3. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT281		low-profile 5-lead TO-220				97-06-11

Flanged ceramic package; 2 mounting holes; 4 leads **SOT289A**

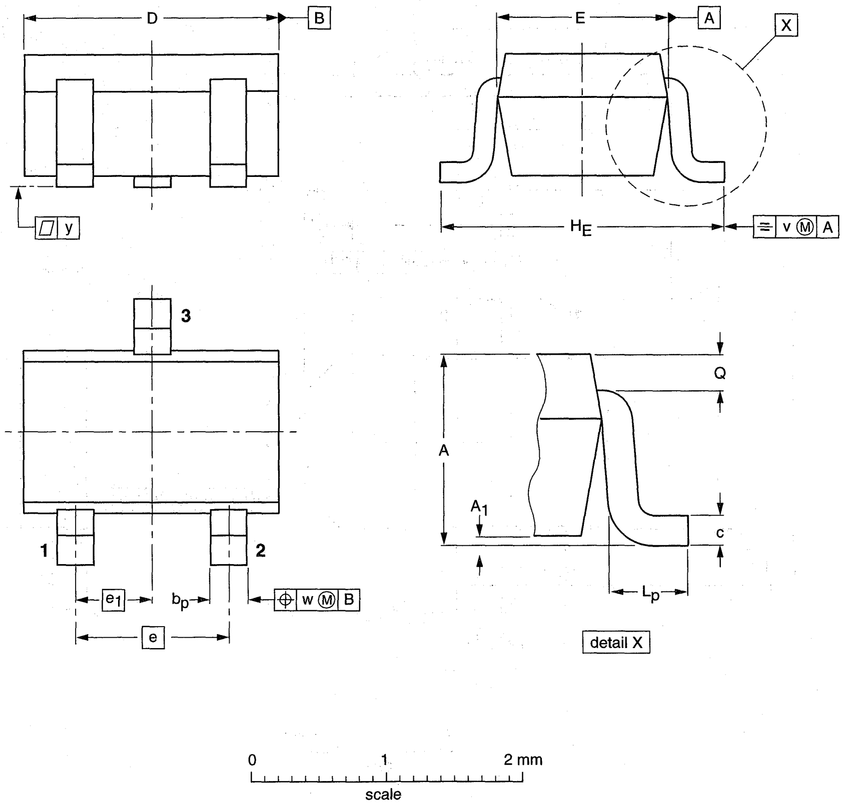


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	4.65 3.92	3.33 3.07	0.10 0.05	13.10 12.90	11.25 11.00	11.53 11.33	4.60	1.65 1.40	19.81 19.05	4.85 4.34	3.43 3.17	2.31 2.06	21.44	28.07 27.81	11.81 11.56	0.51	1.02	0.25
inches	0.183 0.154	0.131 0.121	0.004 0.002	0.516 0.508	0.443 0.433	0.454 0.446	0.181	0.065 0.055	0.780 0.750	0.191 0.171	0.135 0.125	0.091 0.081	0.844	1.105 1.095	0.465 0.455	0.02	0.04	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT289A						99-03-29

Plastic surface mounted package; 3 leads **SOT323**

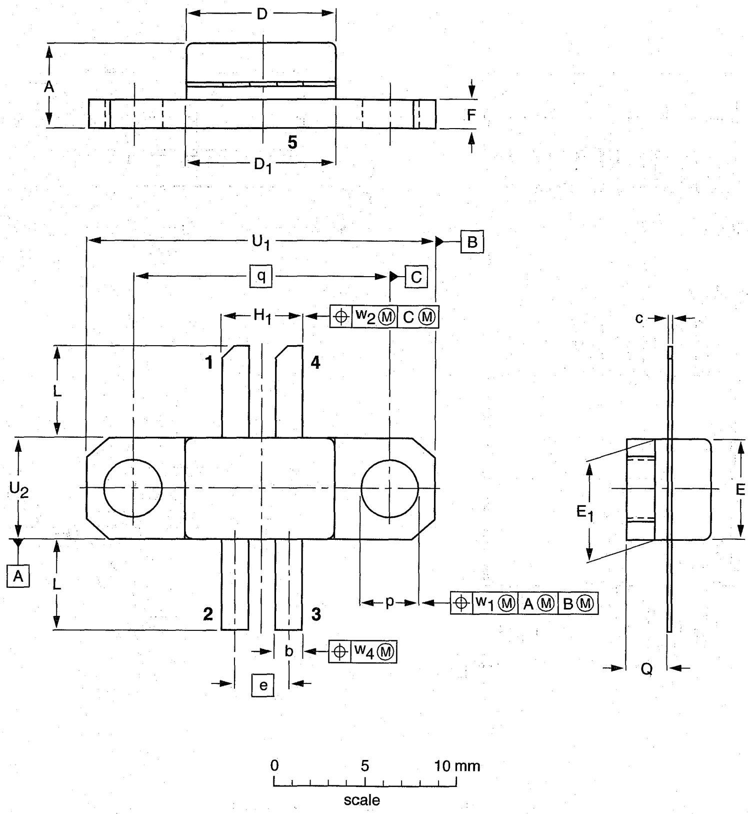


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.1 0.8	0.1	0.4 0.3	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT323			SC-70			97-02-28

Flanged ceramic package; 2 mounting holes; 4 leads **SOT324B**

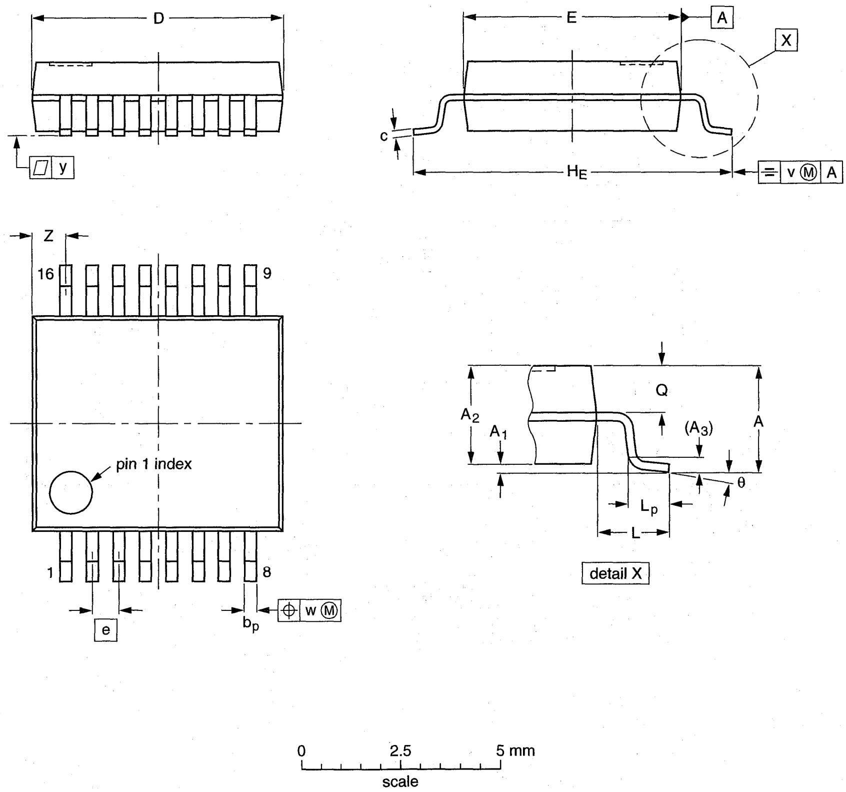


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_4
mm	4.93 4.19	1.65 1.40	0.13 0.08	8.18 8.08	8.26 8.00	6.40 6.30	6.48 6.22	3.05	1.65 1.40	4.83 4.32	5.59 4.57	3.43 3.18	2.31 2.01	14.22	19.02 18.77	6.43 6.17	0.25	0.5	0.25
inches	0.194 0.165	0.065 0.055	0.005 0.003	0.322 0.318	0.325 0.315	0.252 0.248	0.255 0.245	0.120	0.065 0.055	0.19 0.17	0.220 0.180	0.135 0.125	0.091 0.079	0.560	0.749 0.739	0.253 0.243	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT324B						99-03-29

SSOP16: plastic shrink small outline package; 16 leads; body width 5.3 mm **SOT338-1**



DIMENSIONS (mm are the original dimensions)

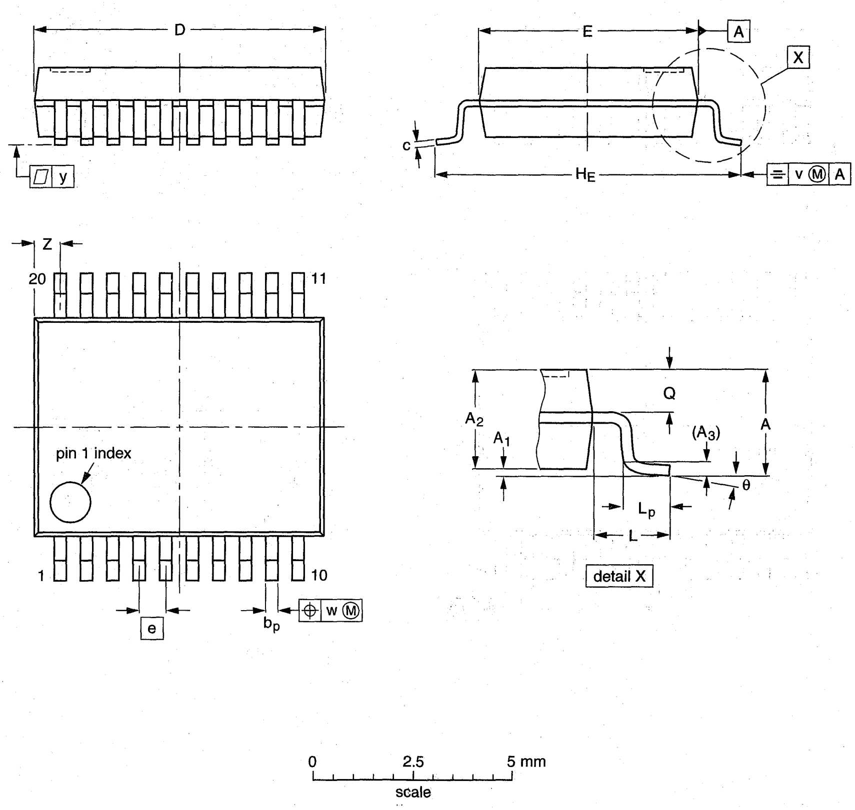
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	6.4 6.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.00 0.55	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT338-1		MO-150AC				~~94-01-14~~ 95-02-04

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm **SOT339-1**



DIMENSIONS (mm are the original dimensions)

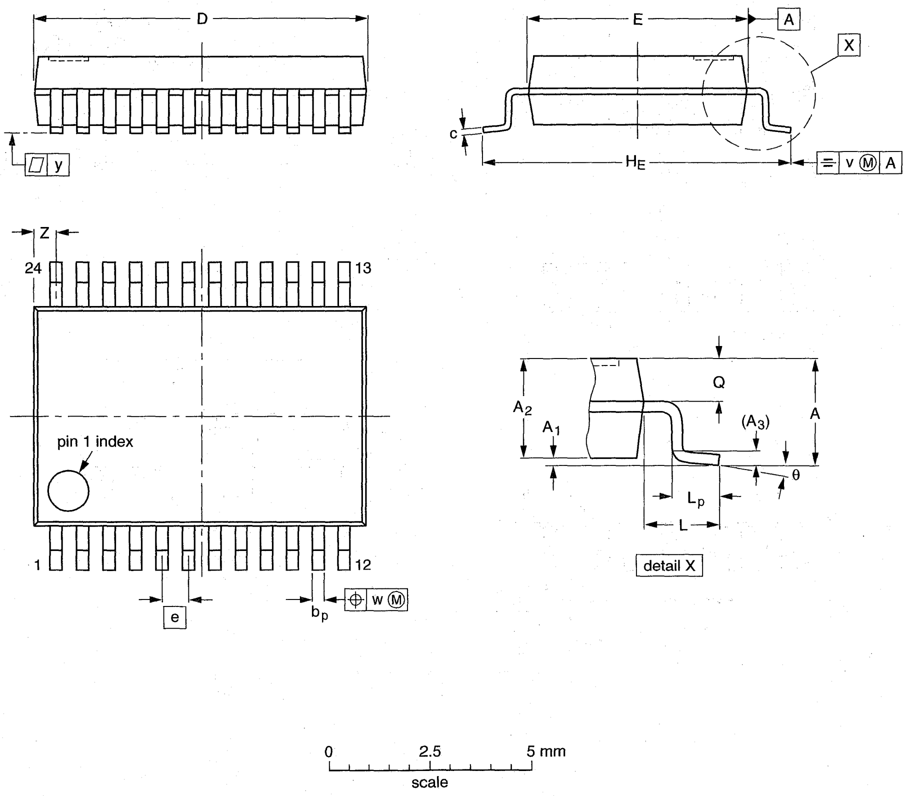
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				~~93-09-08~~ 95-02-04

SSOP24: plastic shrink small outline package; 24 leads; body width 5.3 mm **SOT340-1**



DIMENSIONS (mm are the original dimensions)

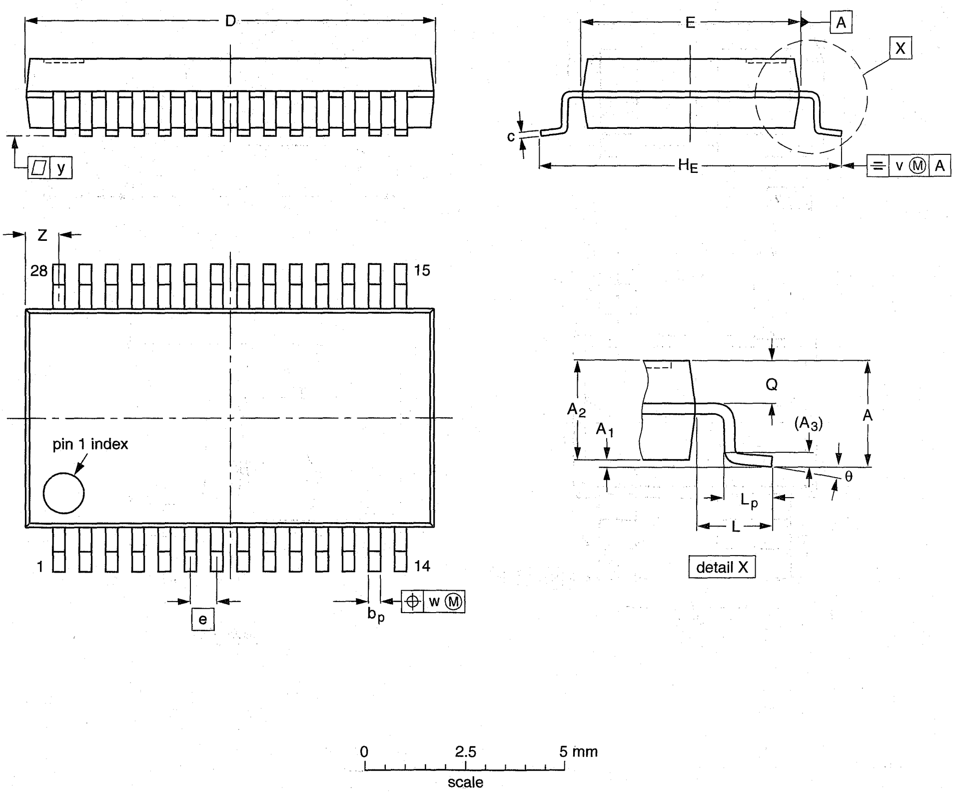
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	8.4 8.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.8 0.4	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT340-1		MO-150AG				~~93-09-08~~ 95-02-04

SSOP28: plastic shrink small outline package; 28 leads; body width 5.3 mm **SOT341-1**



DIMENSIONS (mm are the original dimensions)

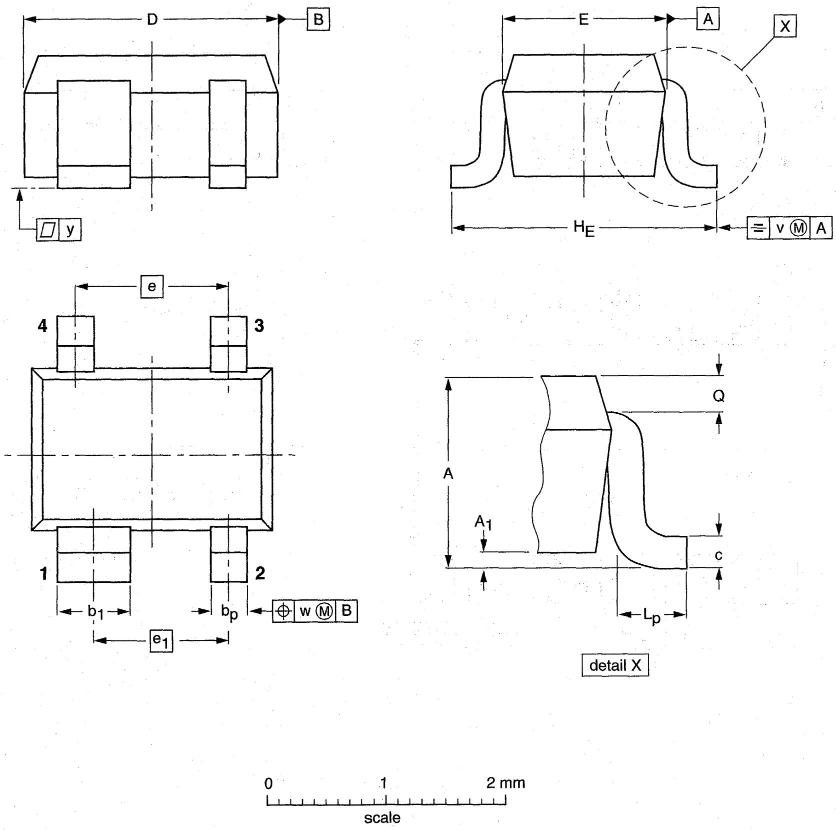
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	10.4 10.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	1.1 0.7	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT341-1		MO-150AH				~~93-09-08~~ 95-02-04

Plastic surface mounted package; 4 leads **SOT343N**

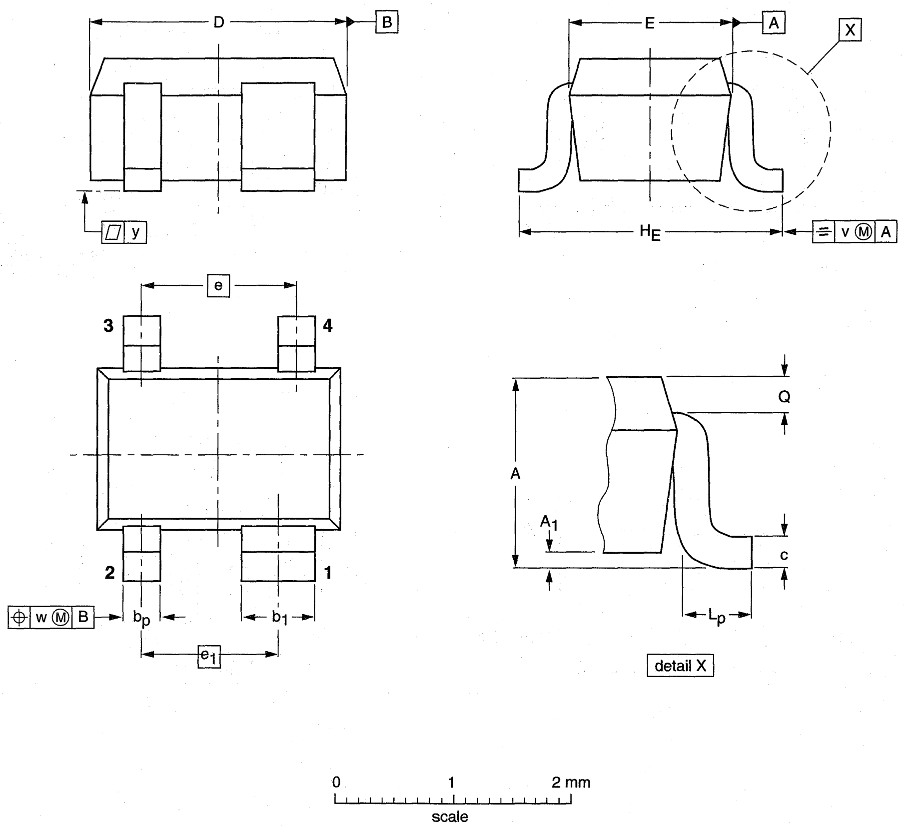


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343N						97-05-21

Plastic surface mounted package; reverse pinning; 4 leads **SOT343R**

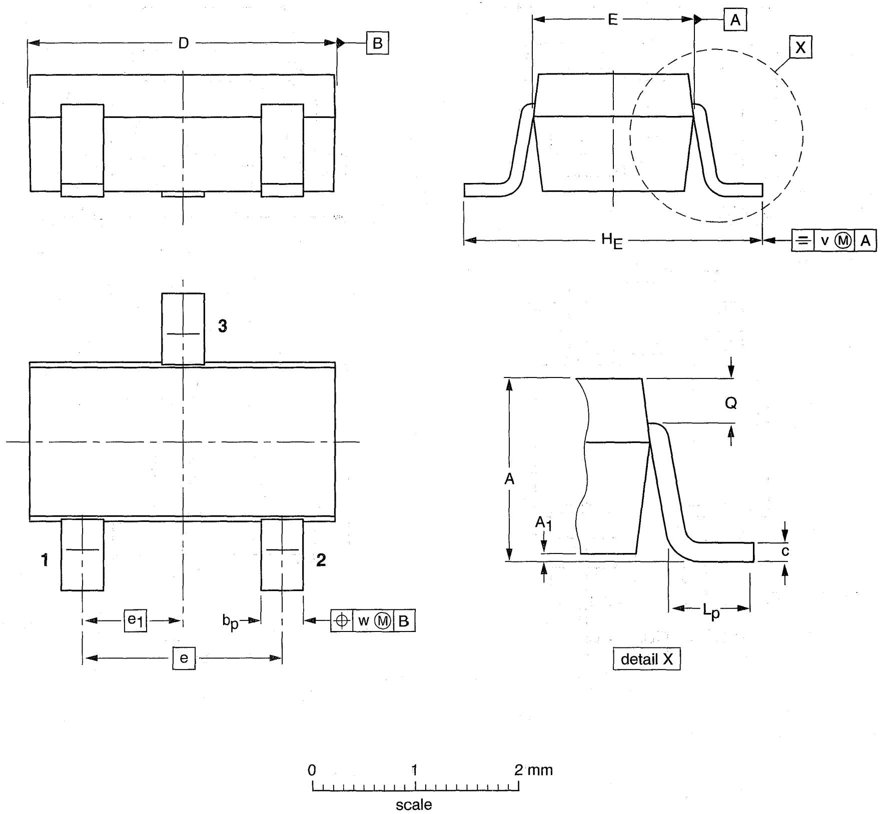


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.4 0.3	0.7 0.5	0.25 0.10	2.2 1.8	1.35 1.15	1.3	1.15	2.2 2.0	0.45 0.15	0.23 0.13	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT343R						97-05-21

Plastic surface mounted package; 3 leads **SOT346**

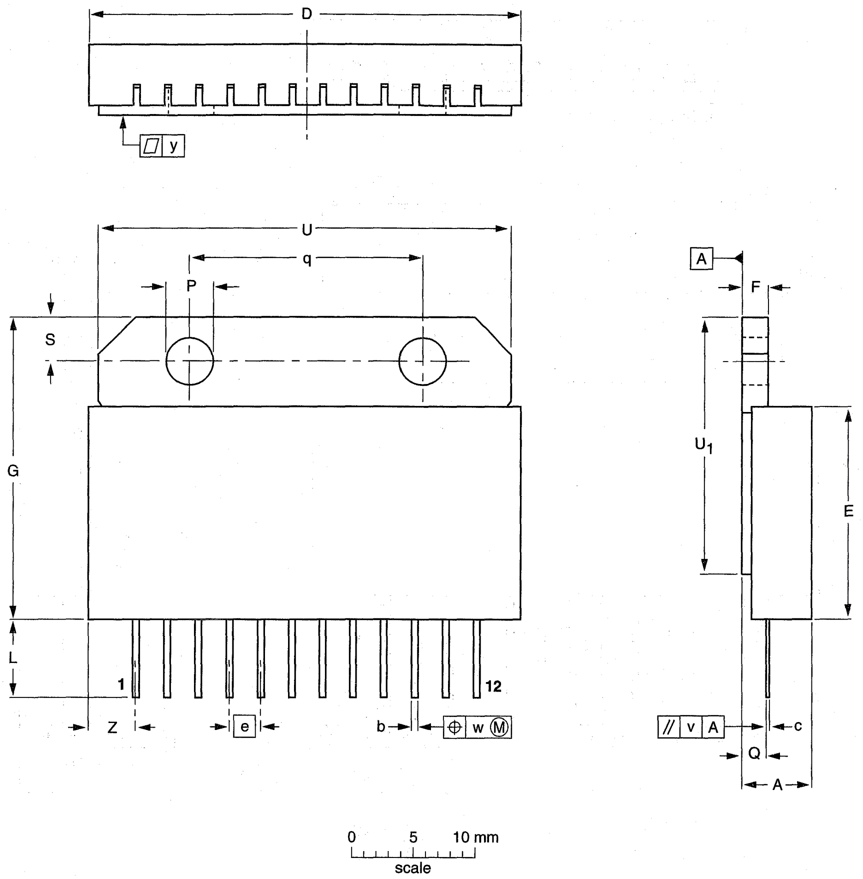


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	1.3 1.0	0.1 0.013	0.50 0.35	0.26 0.10	3.1 2.7	1.7 1.3	1.9	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT346		TO-236	SC-59			98-07-17

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads **SOT347**

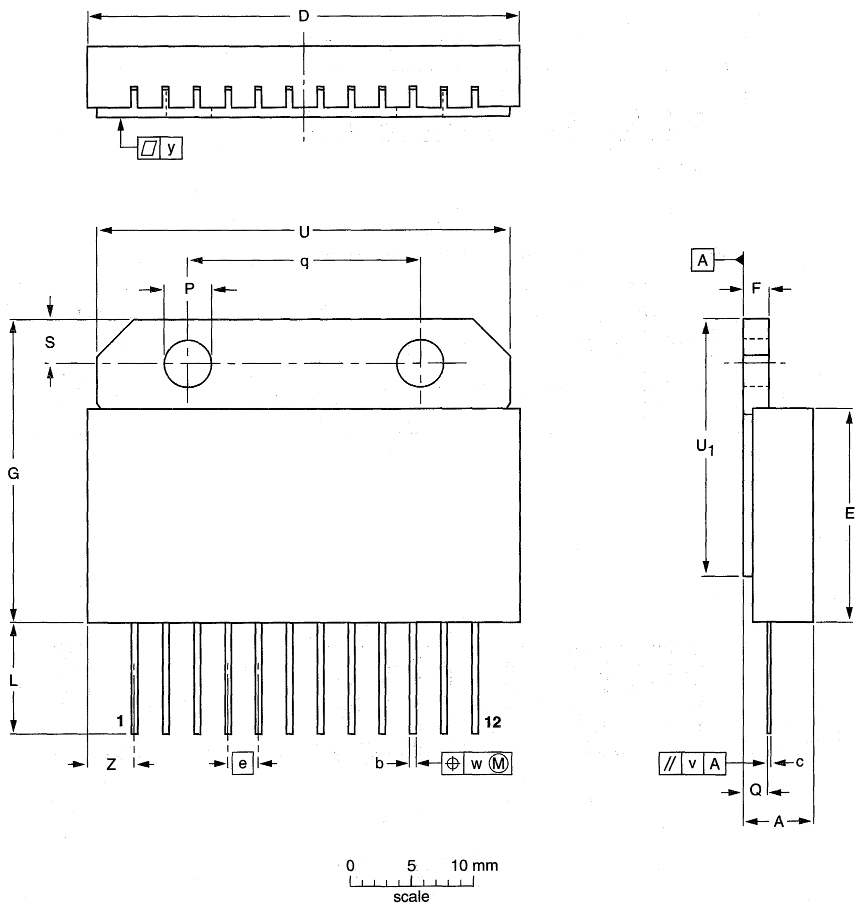


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L min.	P	Q	q	S	U	U_1	v	w	y	Z max.
mm	6.0 5.6	0.51 0.38	0.25	36.2 35.8	18.2 17.8	2.54	2.0	25.5 24.5	6	4.15 3.85	1.8	19	3.5 3.4	34.4 34.0	22.2 21.8	0.3	0.25	0.1	4.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT347						97-06-28

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads **SOT347B**

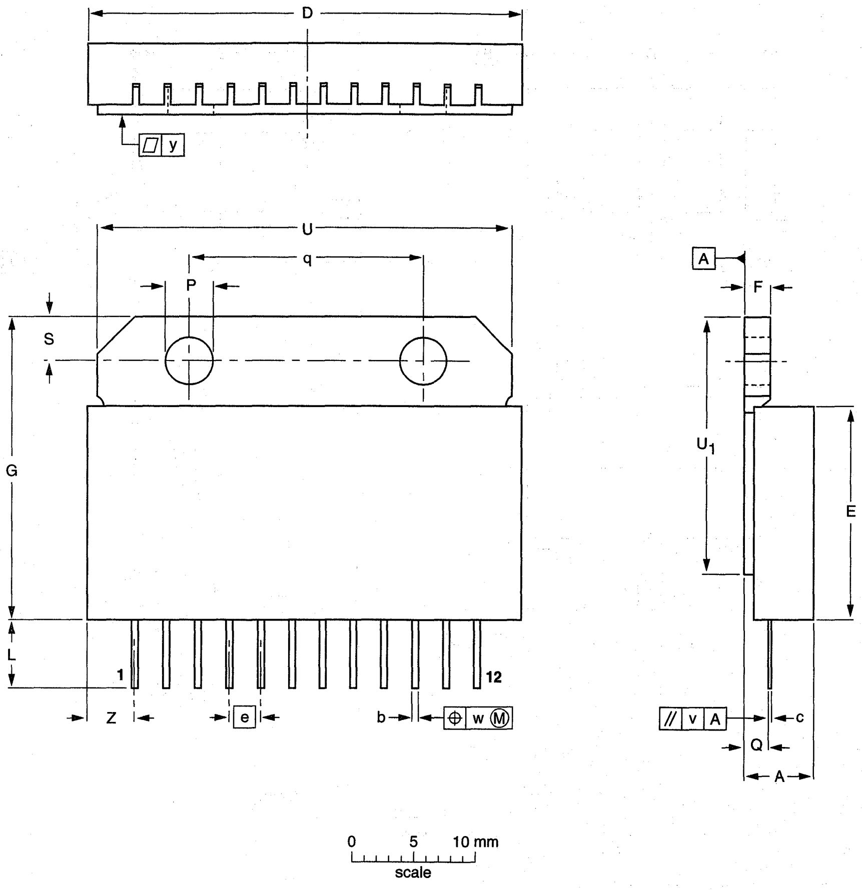


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L min.	P	Q	q	S	U	U_1	v	w	y	Z max.
mm	6.0 5.6	0.51 0.38	0.25	36.2 35.8	18.2 17.8	2.54	2.0	25.5 24.5	9	4.15 3.85	1.8	19	3.5 3.4	34.4 34.0	22.2 21.8	0.3	0.25	0.1	4.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT347B						99-01-05

Ceramic single-ended flat package; heatsink mounted; 2 mounting holes; 12 in-line tin (Sn) plated leads **SOT347C**

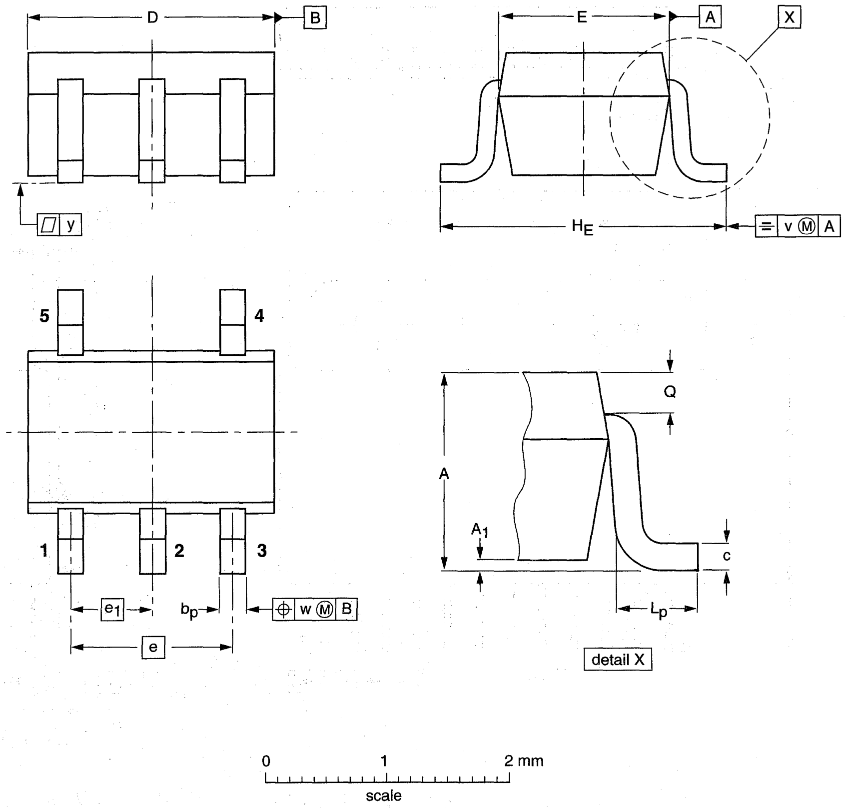


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L	P	Q	q	S	U	U_1	v	w	y	Z max.
mm	6.0 5.6	0.51 0.38	0.25	36.2 35.8	18.2 17.8	2.54	2.0	25.5 24.5	5.9 5.3	4.15 3.85	2.05 1.55	19.2 18.8	3.5 3.4	34.4 34.0	22.2 21.8	0.3	0.25	0.1	4.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT347C						99-01-05

Plastic surface mounted package; 5 leads **SOT353**

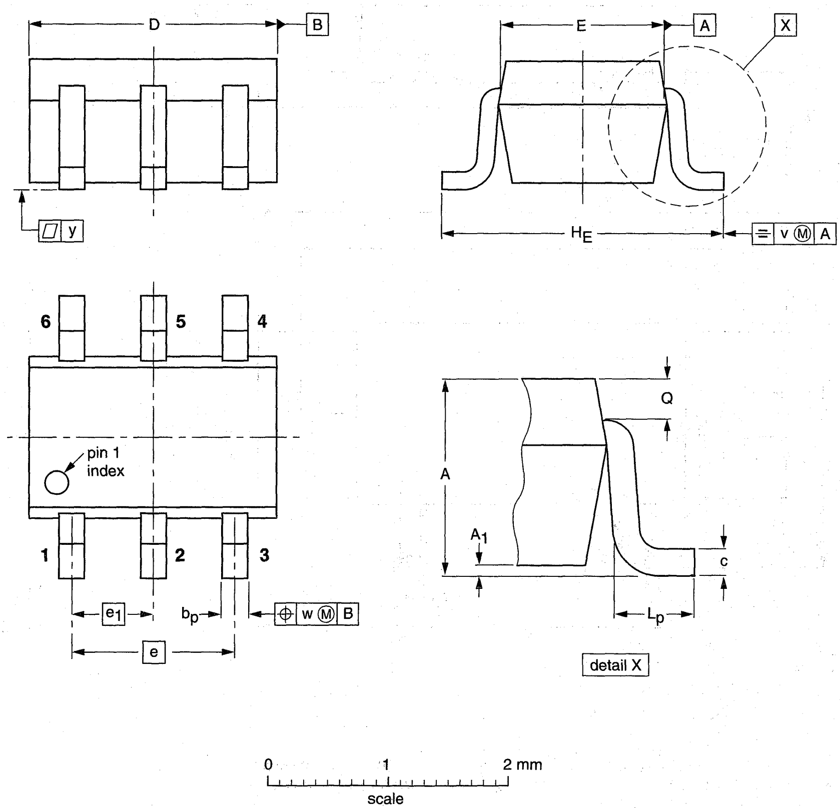


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E (2)	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

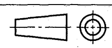
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT353			SC-88A			97-02-28

Plastic surface mounted package; 6 leads **SOT363**

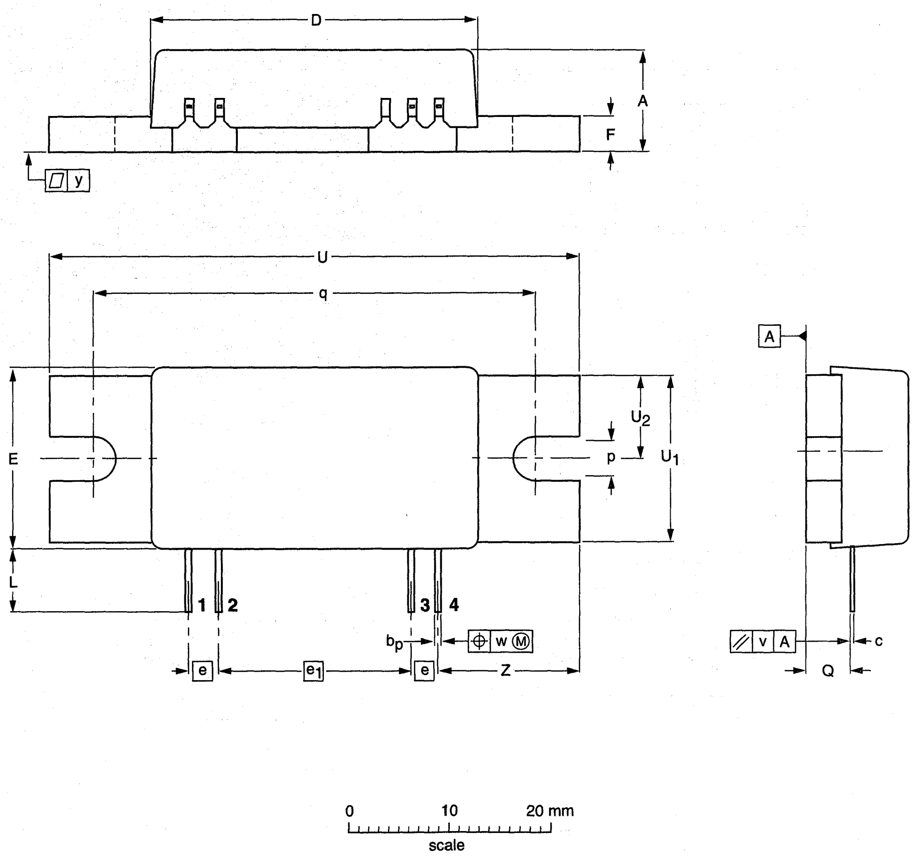


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w	y
mm	1.1 0.8	0.1	0.30 0.20	0.25 0.10	2.2 1.8	1.35 1.15	1.3	0.65	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT363			SC-88			97-02-28

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads SOT365A

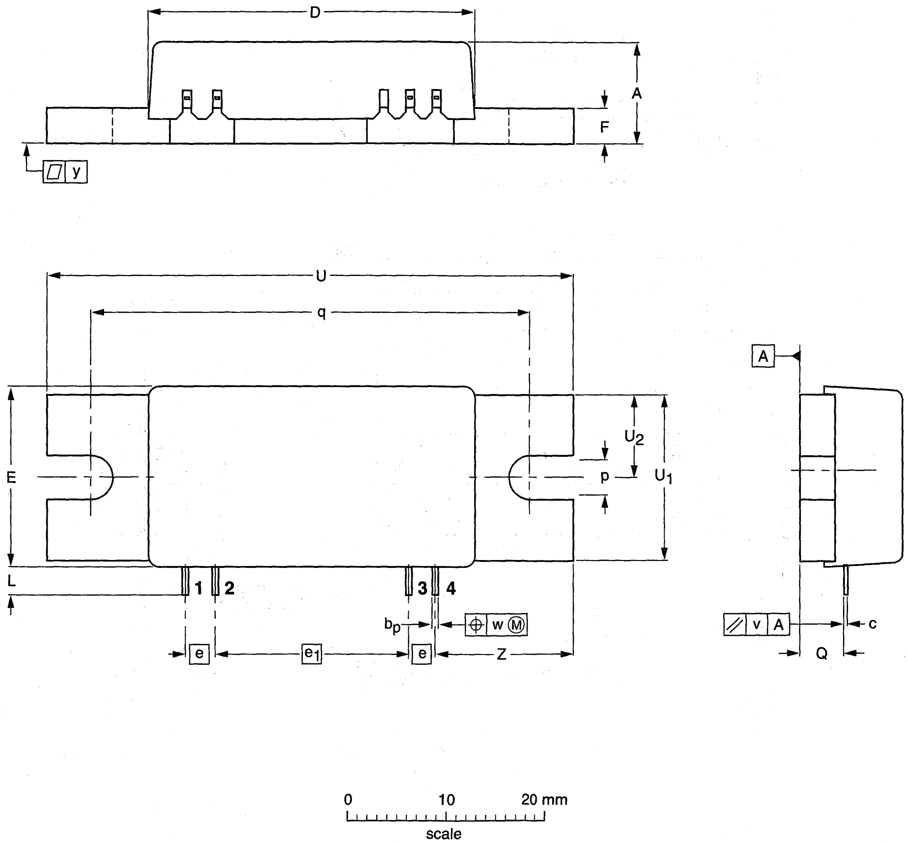


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	F	L	p	Q	q	U	U_1	U_2	v	w	y	Z
mm	9.5 9.0	0.56 0.46	0.3 0.2	30.1 29.9	18.6 18.4	2.54	17.78	3.25 3.15	6.5 6.1	4.1 3.9	4.0 3.8	40.74 40.54	48.0 48.4	15.4 15.2	7.75 7.55	0.3	0.25	0.1	12.8 12.6

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT365A						99-02-06

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads SOT365B

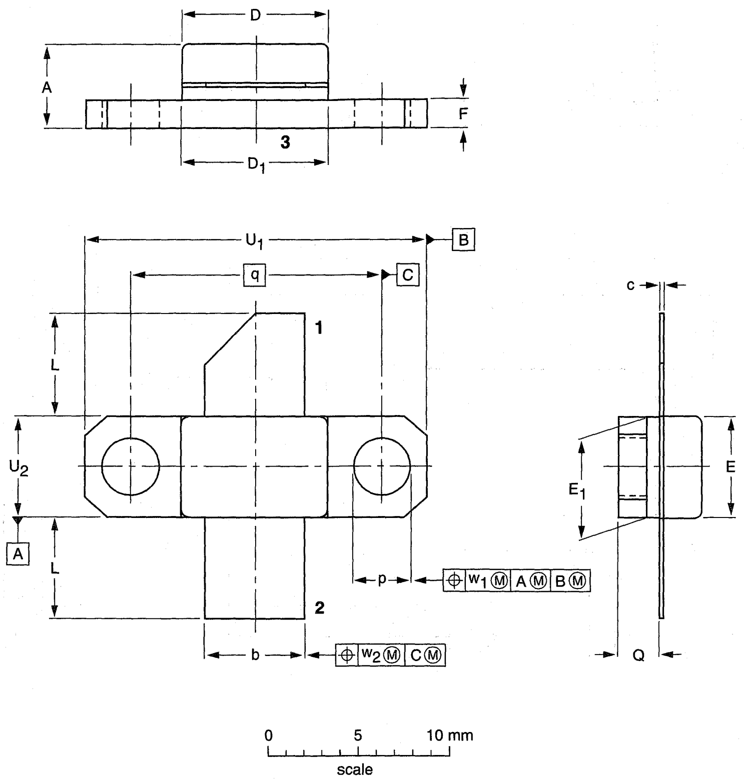


DIMENSIONS (mm are the original dimensions)

UNIT	A	b_p	c	D	E	e	e_1	F	L	p	Q	q	U	U_1	U_2	v	w	y	Z
mm	9.5 9.0	0.56 0.46	0.3 0.2	30.1 29.9	18.6 18.4	2.54	17.78	3.25 3.15	2.8 2.3	4.1 3.9	4.0 3.8	40.74 40.54	48.0 48.4	15.4 15.2	7.75 7.55	0.3	0.25	0.1	12.8 12.6

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT365B						99-02-06

Flanged ceramic package; 2 mounting holes; 2 leads **SOT390A**

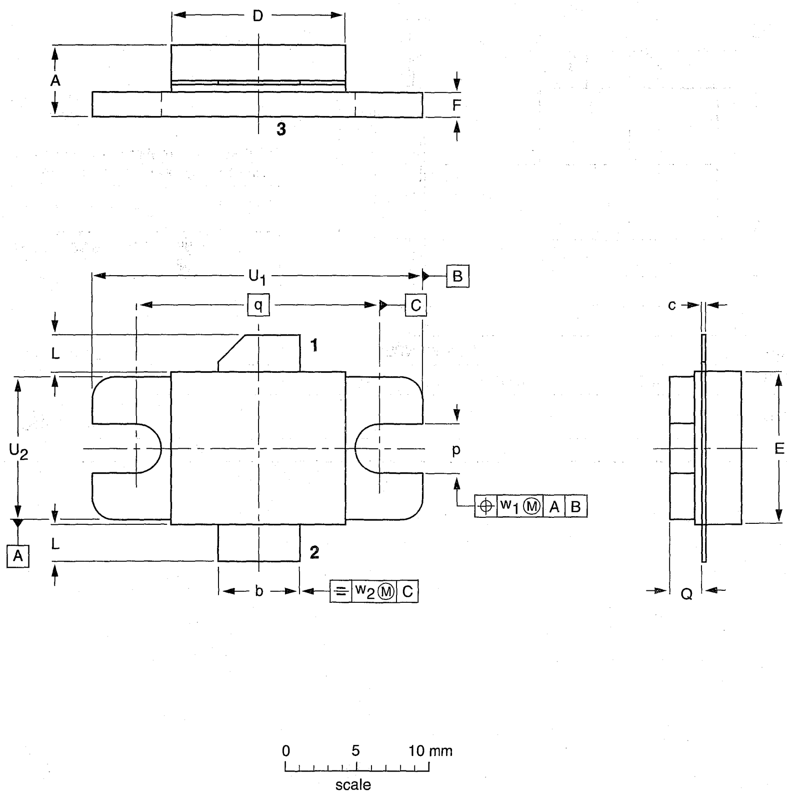


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.03 4.22	5.72 5.46	0.16 0.10	8.18 8.08	8.26 8.00	6.40 6.30	6.43 6.17	1.66 1.39	6.10 5.33	3.43 3.17	2.32 2.00	14.22	19.03 18.77	6.43 6.17	0.25	0.51
inches	0.198 0.166	0.225 0.215	0.006 0.004	0.322 0.318	0.325 0.315	0.252 0.248	0.253 0.243	0.065 0.055	0.24 0.21	0.135 0.125	0.091 0.079	0.560	0.749 0.739	0.253 0.243	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT390A						99-03-29

Flanged ceramic package; 2 mounting holes; 2 leads **SOT391A**

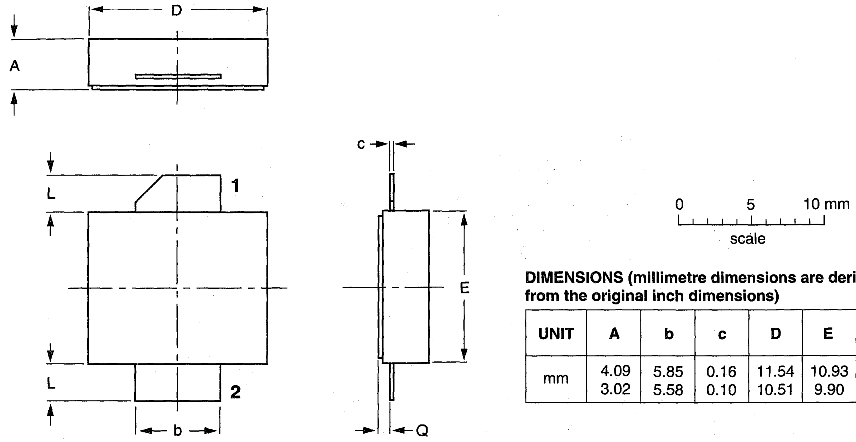


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.36 4.29	5.85 5.58	0.16 0.10	11.54 10.51	10.93 9.90	1.66 1.39	2.79 2.29	3.43 3.17	2.29 2.03	16.51	22.99 22.73	9.91 9.65	0.51	1.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391A						97-05-29

Flangeless ceramic package; 2 leads | SOT391B

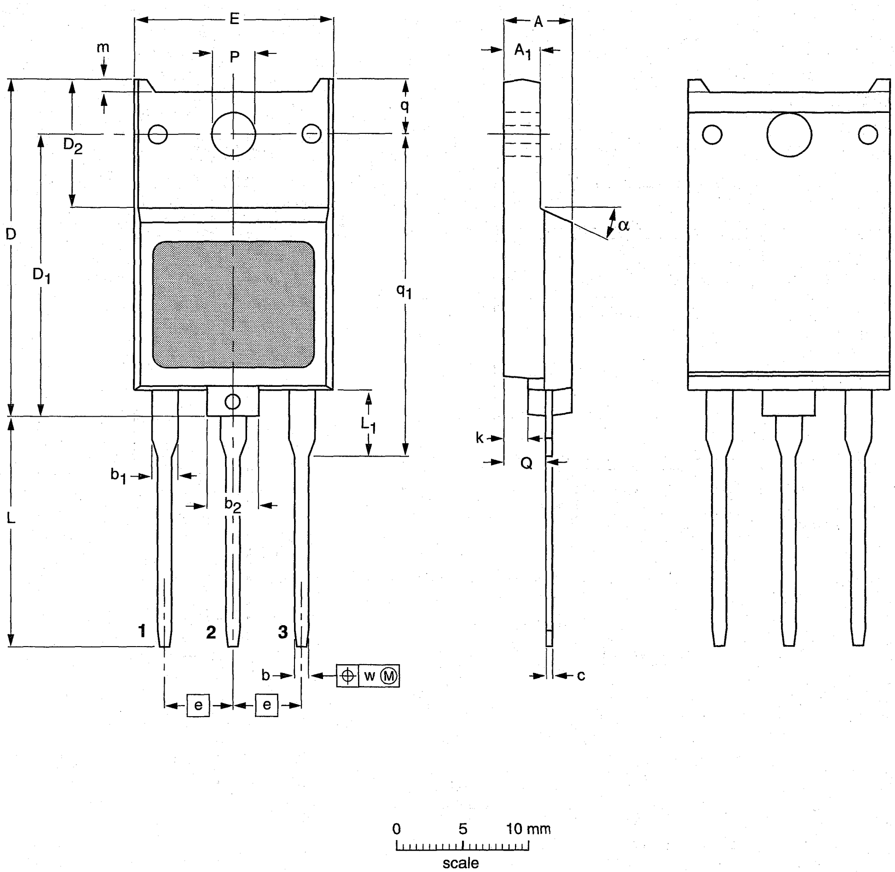


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	L	Q
mm	4.09 3.02	5.85 5.58	0.16 0.10	11.54 10.51	10.93 9.90	2.79 2.29	1.02 0.76

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391B						97-05-29

Plastic single-ended through-hole package; mountable to heatsink; 1 mounting hole; 3 in-line leads SOT399



DIMENSIONS (mm are the original dimensions)

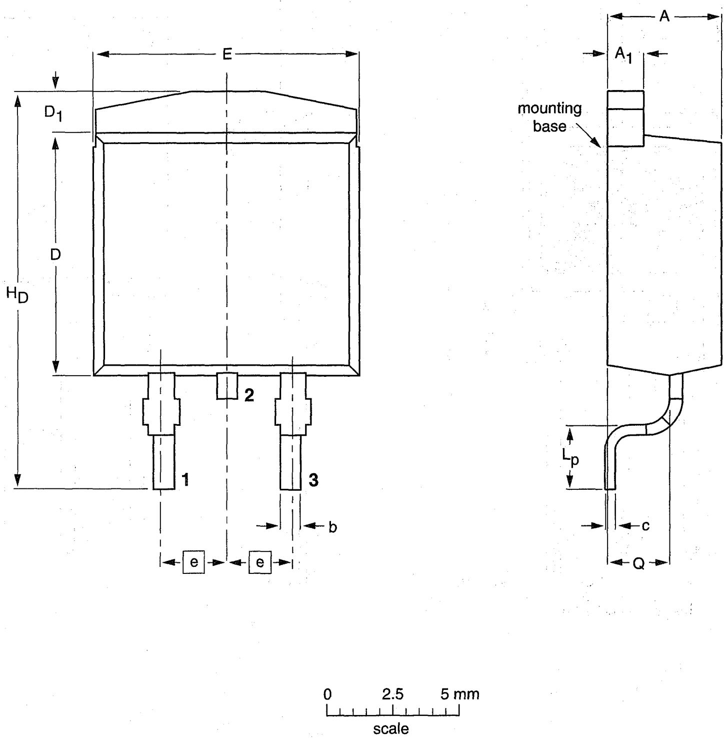
UNIT	A	A_1	b	b_1	b_2	c	D	D_1	D_2	E	e	k	L	L_1(1)	m	P	Q	q	q_1	w	α
mm	5.8 4.8	3.3 2.7	1.2 0.9	2.2 1.8	4.7 4.2	0.9 0.6	27 26	22.5 21.5	10.2 9.9	16 15	5.45	2.2 1.8	19.1 18.1	5.4 4.8	0.8 0.6	3.4 3.1	3.4 3.2	4.7 4.3	25.7 25.1	0.4	27° 23°

Note

1. Tinning of terminals are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT399						98-11-06

Plastic single-ended surface mounted package (Philips version of D2-PAK); 3 leads (one lead cropped) **SOT404**

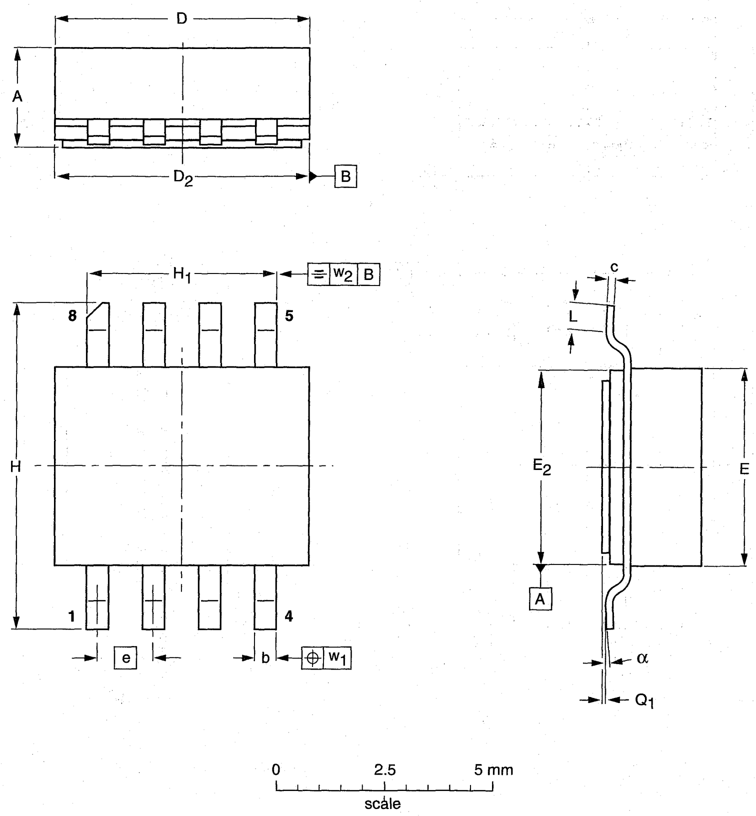


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	e	L_p	H_D	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	0.64 0.46	9.65 8.65	1.6 1.2	10.3 9.7	2.54	2.9 2.1	15.4 14.8	2.60 2.20

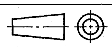
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						98-12-14

Ceramic surface mounted package; 8 leads **SOT409A**

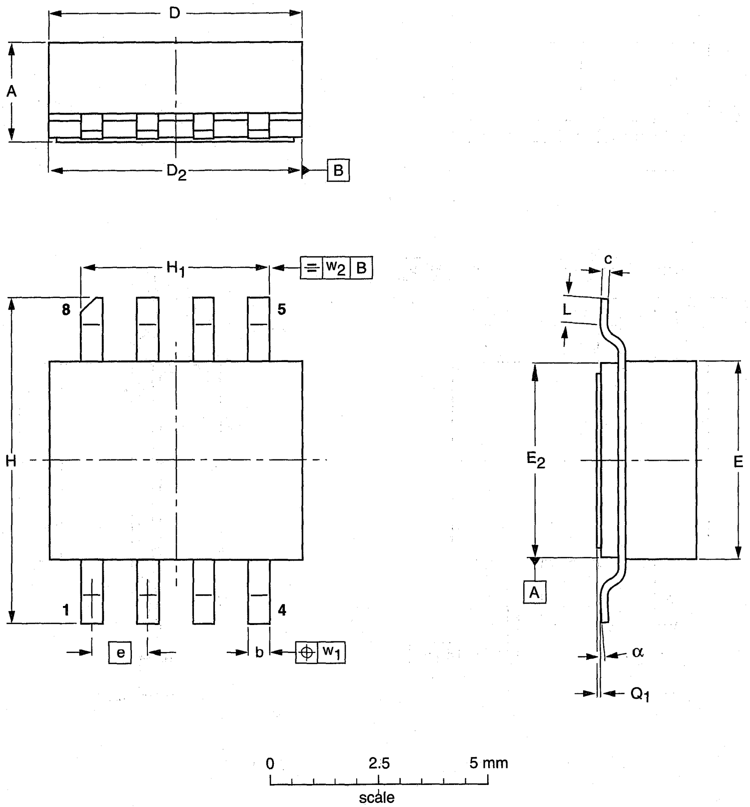


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						98-01-27

Ceramic surface mounted package; 8 leads — SOT409B

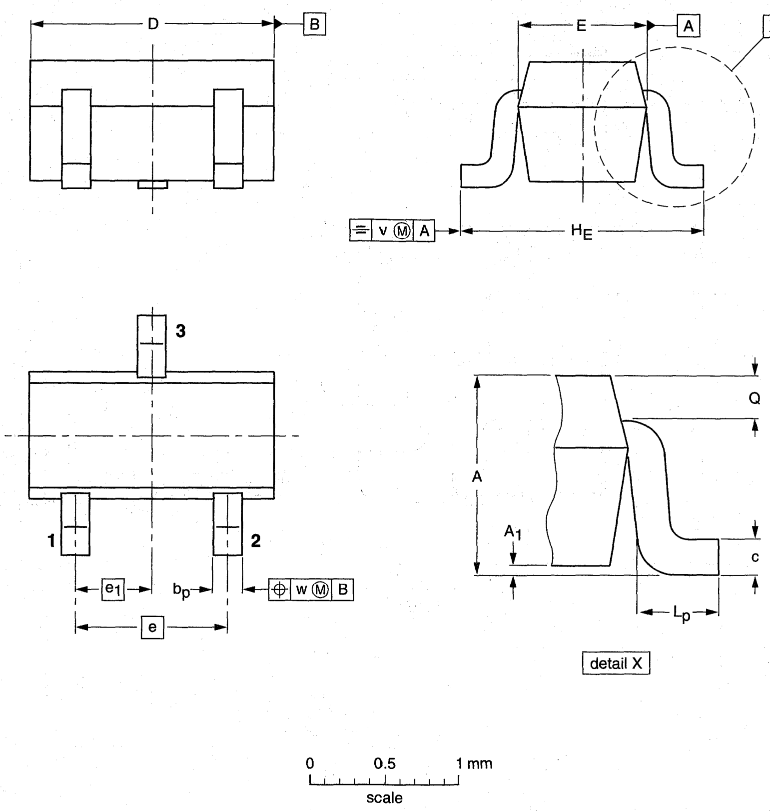


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.15 0.10	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	0.84 0.69	0.10 0.00	0.25	0.25	2° 0°
inches	0.093 0.081	0.023 0.017	0.006 0.004	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.033 0.027	0.004 0.000	0.010	0.010	2° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409B						98-01-27

Plastic surface mounted package; 3 leads **SOT416**

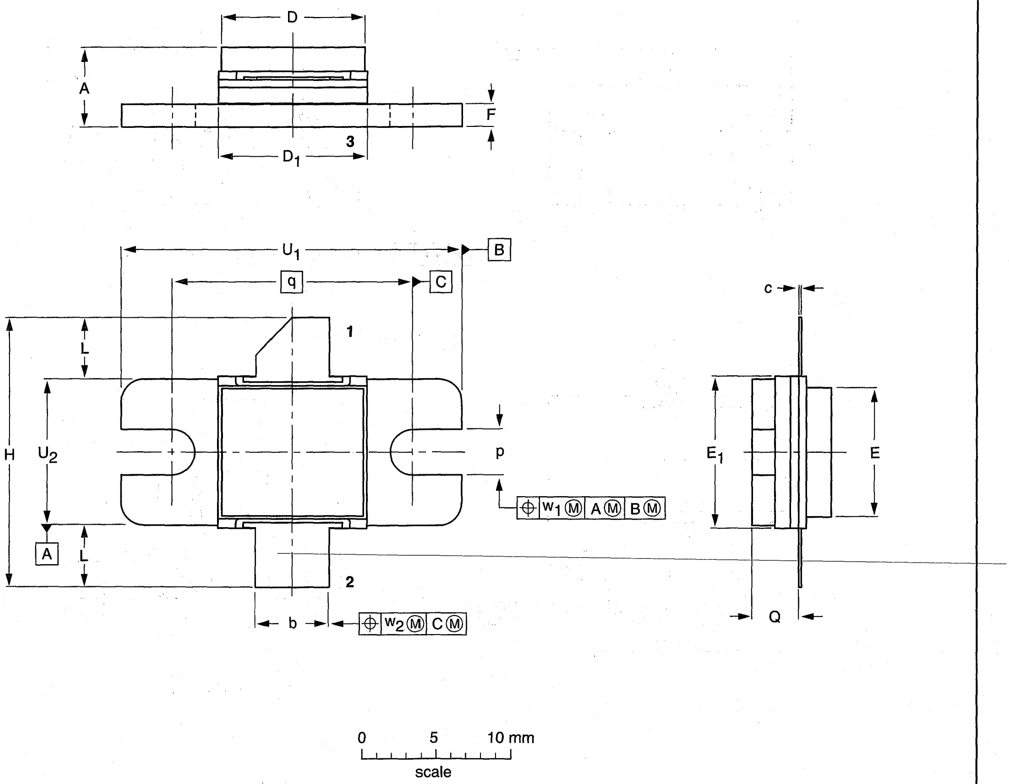


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	c	D	E	e	e_1	H_E	L_p	Q	v	w
mm	0.95 0.60	0.1	0.30 0.15	0.25 0.10	1.8 1.4	0.9 0.7	1	0.5	1.75 1.45	0.45 0.15	0.23 0.13	0.2	0.2

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT416			SC-75			97-02-28

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT422A**

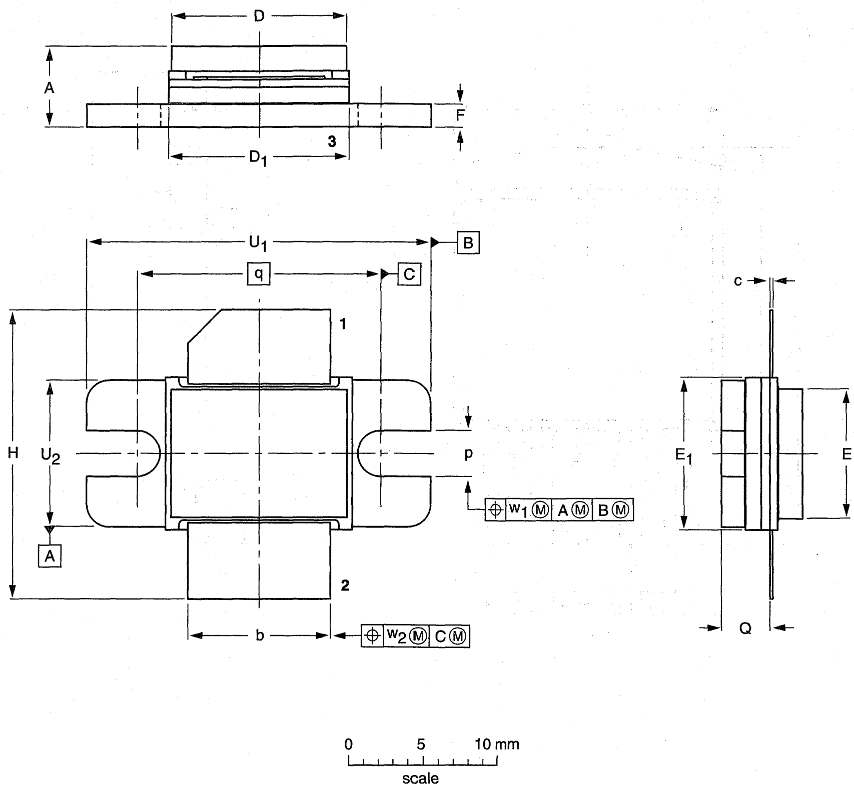


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.72 4.83	5.21 4.95	0.13 0.08	9.93 9.68	10.29 10.03	8.76 8.51	10.29 10.03	1.58 1.47	19.18 17.65	4.52 3.74	3.43 3.18	3.35 2.92	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.190	0.205 0.195	0.005 0.003	0.391 0.381	0.405 0.395	0.345 0.335	0.405 0.395	0.062 0.058	0.755 0.695	0.178 0.147	0.135 0.125	0.132 0.115	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT422A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT423A**

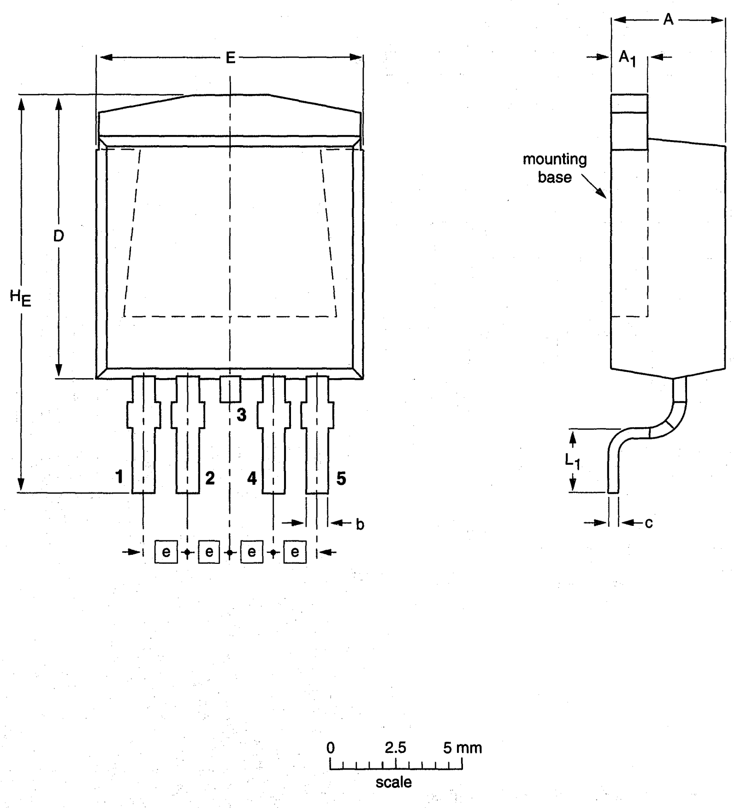


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.72 4.90	9.53 9.27	0.10 0.05	12.09 11.71	12.83 12.57	8.84 8.56	10.29 10.03	1.58 1.47	19.81 18.29	3.43 3.18	3.35 2.95	16.51	22.99 22.73	9.91 9.65	0.25	0.76
inches	0.225 0.193	0.375 0.365	0.004 0.002	0.476 0.461	0.505 0.495	0.348 0.337	0.405 0.395	0.062 0.058	0.78 0.72	0.135 0.125	0.132 0.116	0.65	0.905 0.895	0.390 0.380	0.01	0.03

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT423A						99-03-29

Plastic single-ended surface mounted package (Philips version of D^2-PAK); 5 leads (one lead cropped) **SOT426**

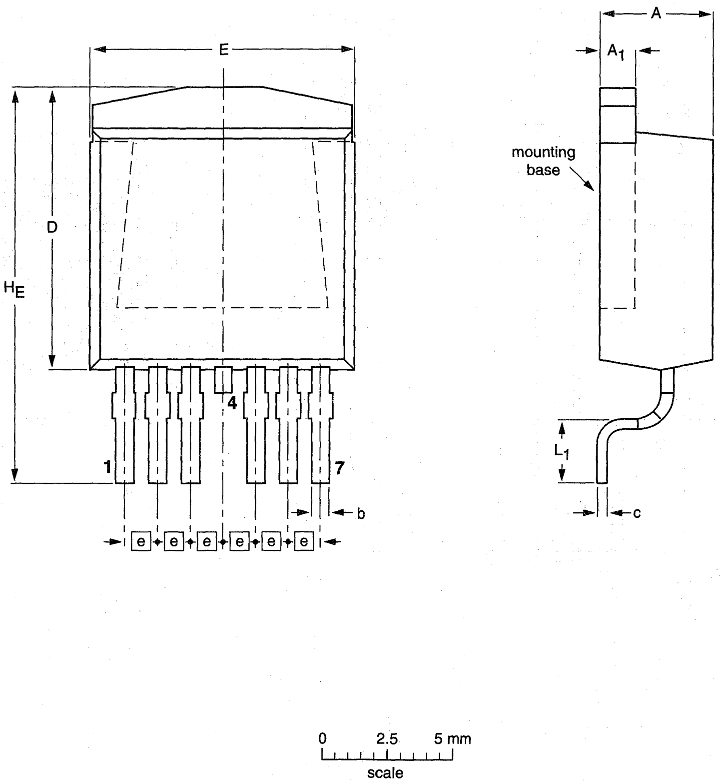


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	E	e	L_1	H_E
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	10.30 9.70	1.70	2.90 2.10	15.80 14.80

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT426						98-12-14

Plastic single-ended suface mounted package (Philips version of D²-PAK); 7 leads (one lead cropped) **SOT427**

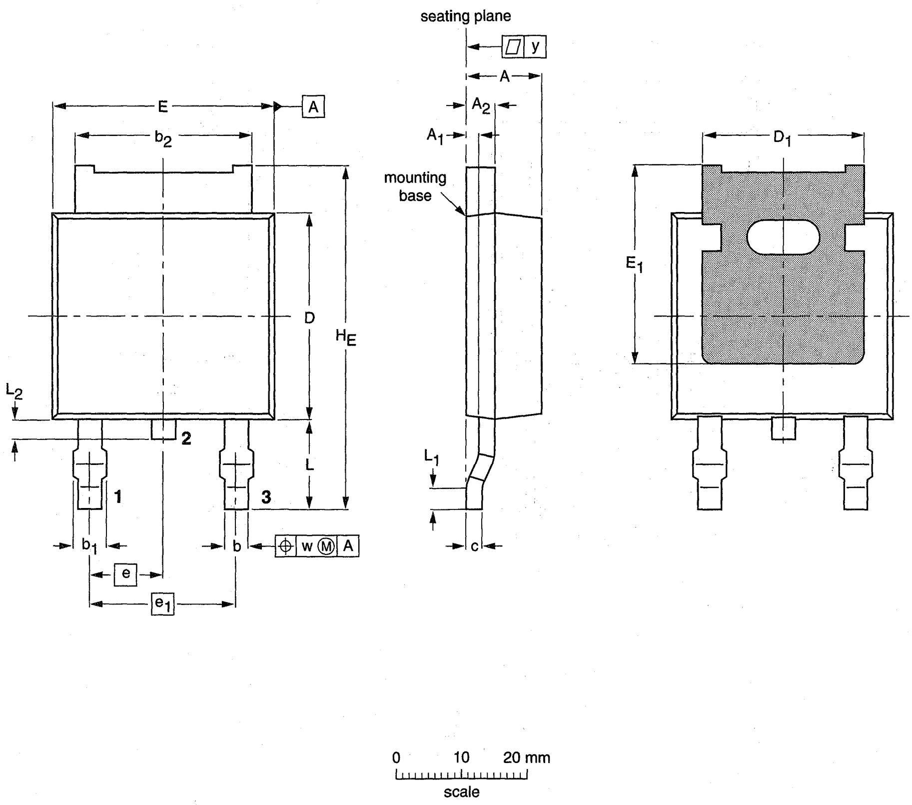


DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	E	e	L_1	H_E
mm	4.50 4.10	1.40 1.27	0.7 0.4	0.64 0.46	11	10.30 9.70	1.27	2.90 2.10	15.80 14.80

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT427						98-12-14

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped) **SOT428**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	$A_1^{(1)}$	A_2	b	b_1 max.	b_2	c	D max.	D_1 max.	E max.	E_1 min.	e	e_1	H_E max.	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.89 0.71	0.89 0.71	1.1 0.9	5.36 5.26	0.4 0.2	6.22 5.98	4.81 4.45	6.73 6.47	4.0	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.7 0.5	0.2	0.2

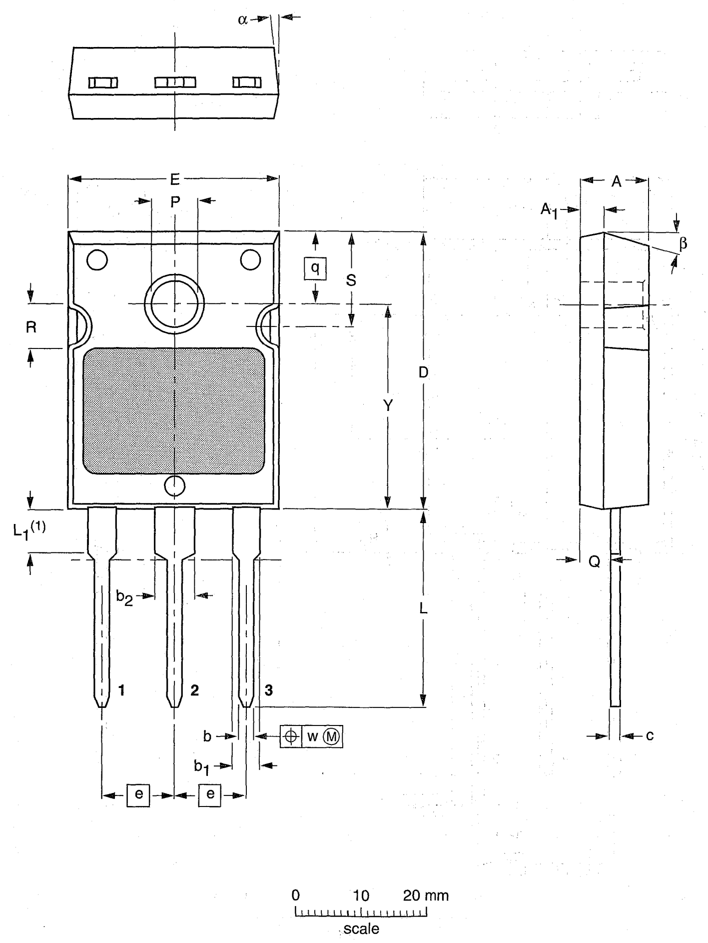
Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT428						98-04-07

Package outlines Chapter 2

Plastic single-ended through-hole package; heatsink mounted; 1 mounting hole; 3-lead TO-247 **SOT429**



DIMENSIONS (mm are the original dimensions)

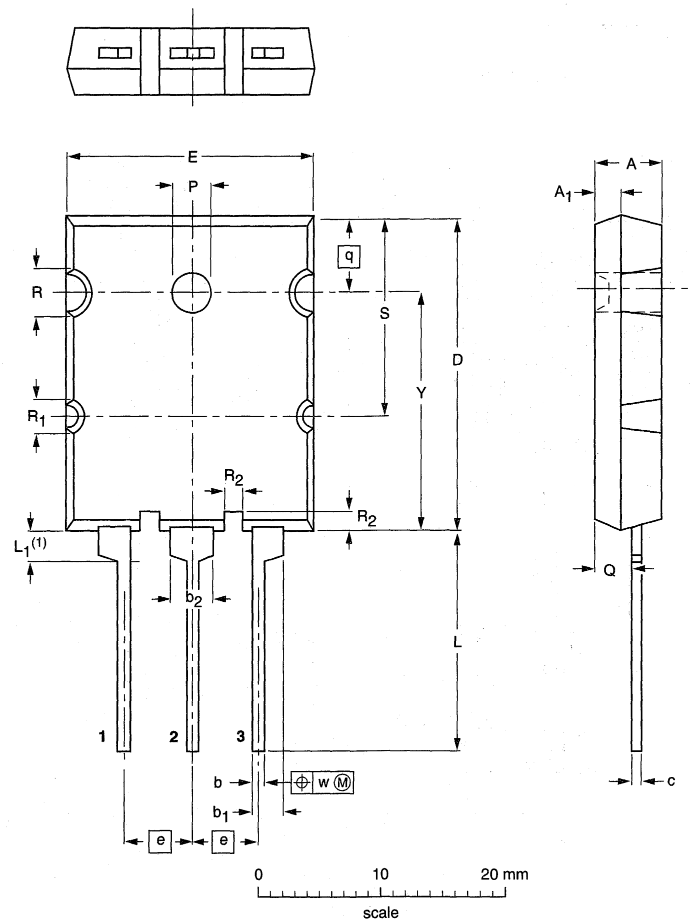
UNIT	A	A_1	b	b_1	b_2	c	D	E	e	L	$L_1^{(1)}$	P	Q	q	R	S	w	Y	α	β
mm	5.3 4.7	1.9 1.7	1.2 0.9	2.2 1.8	3.2 2.8	0.9 0.6	21 20	16 15	5.45	16 15	4.0 3.6	3.7 3.3	2.6 2.4	5.3	3.5 3.3	7.5 7.1	0.4	15.7 15.3	6° 4°	17° 13°

Note

1. Tinning of terminals are uncontrolled within zone L_1.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT429		TO-247				98-04-07

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead JUMBO TO-247 **SOT430**



DIMENSIONS (mm are the original dimensions)

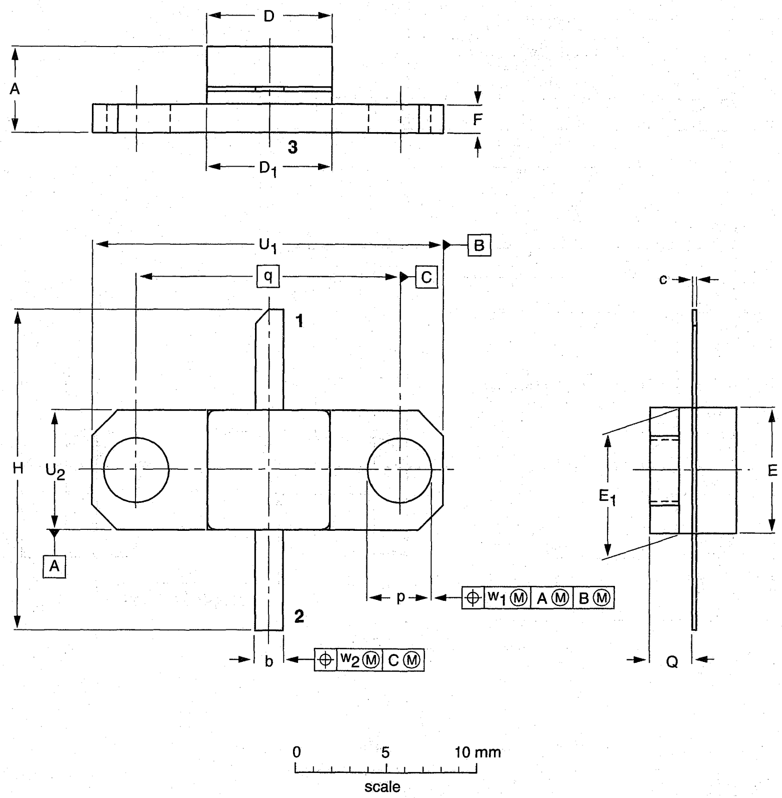
UNIT	A max.	A_1	b	b_1 max.	b_2 max.	c max.	D	E max.	e	L min.	L_1	P	Q max.	q	R	R_1	R_2	S	w	Y
mm	5.3	2.3	1.0 0.8	2.5	3.5	0.8	26.5 25.5	20.5	5.45	19.5	2.5	3.5 3.1	3.0	6.0	4.0	3.0	1.5	16	0.4	20.5 19.5

Note

1. Terminals are uncontrolled within zone L_1.

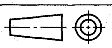
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT430						97-06-23

Flanged ceramic package; 2 mounting holes; 2 leads SOT437A

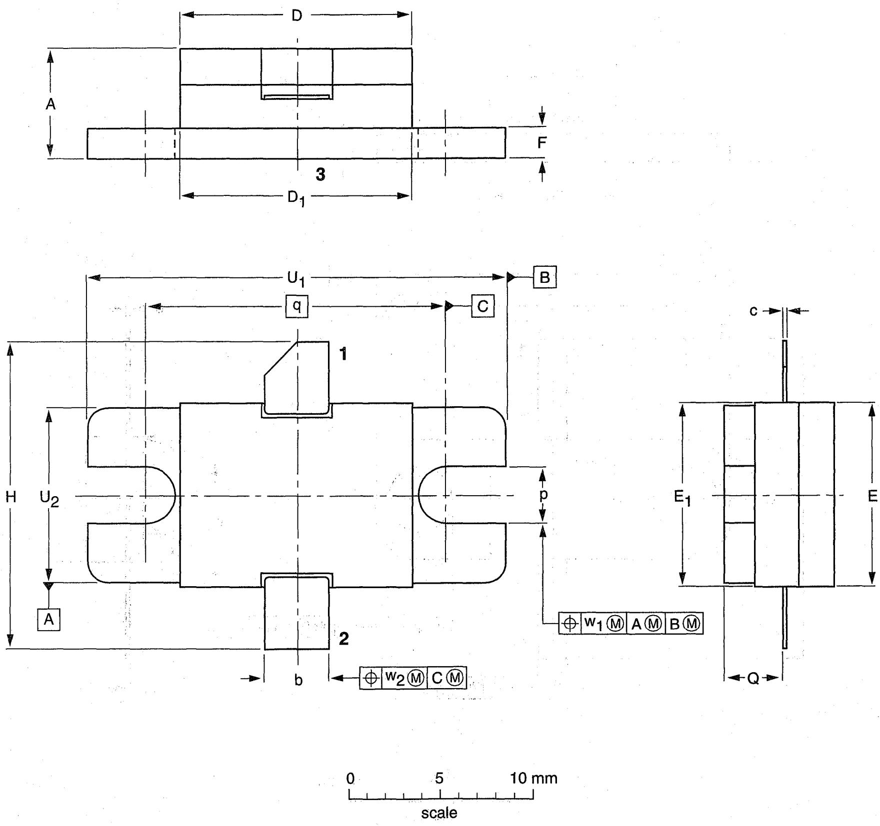


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.98 4.32	1.66 1.40	0.13 0.08	6.48 6.22	6.48 6.22	6.48 6.22	6.48 6.22	1.65 1.40	17.02 16.00	3.43 3.18	2.29 2.03	14.22	19.02 18.77	6.48 6.22	0.25	0.51
inches	0.196 0.170	0.065 0.055	0.005 0.003	0.255 0.245	0.255 0.245	0.255 0.245	0.255 0.245	0.065 0.055	0.67 0.63	0.135 0.125	0.90 0.80	0.560	0.749 0.739	0.255 0.245	0.010	0.020

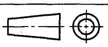
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT437A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads — SOT439A

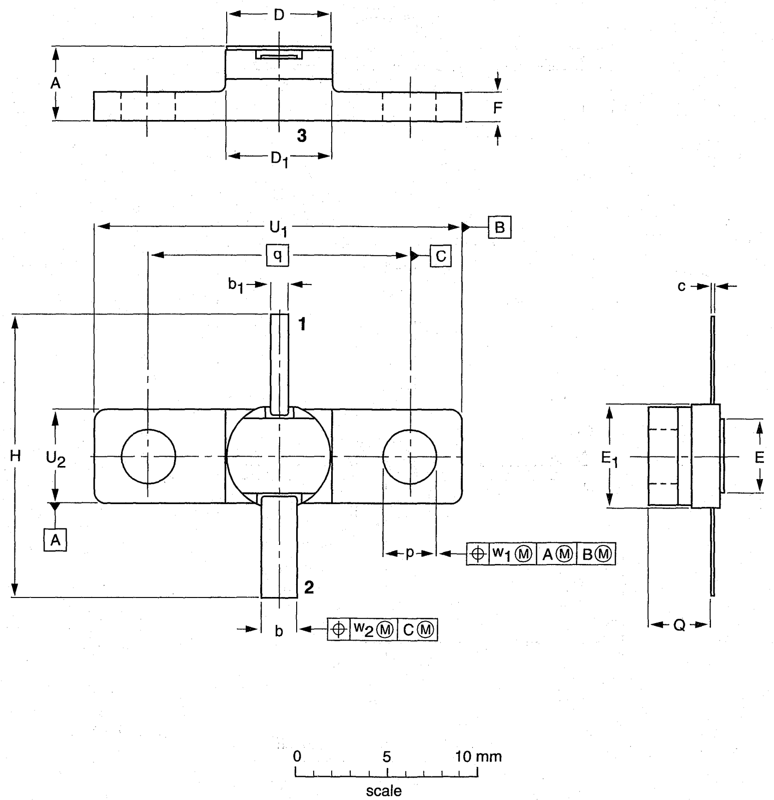


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	6.05 5.23	3.69 3.42	0.13 0.05	12.85 12.55	12.83 12.57	10.31 10.01	10.26 10.06	1.58 1.47	17.27 15.75	3.43 3.17	3.33 2.97	16.51	22.94 22.73	9.91 9.65	0.25	0.79
inches	0.238 0.206	0.145 0.135	0.005 0.002	0.506 0.494	0.505 0.495	0.406 0.394	0.404 0.396	0.62 0.58	0.680 0.620	0.135 0.125	0.131 0.117	0.650	0.905 0.895	0.390 0.380	0.010	0.031

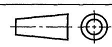
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT439A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT440A**

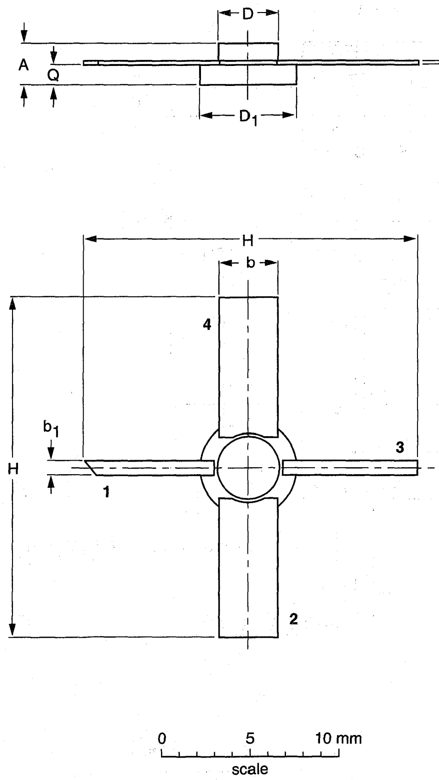


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	b_1	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.25 3.32	2.16 1.90	1.15 0.89	0.14 0.09	5.70 5.50	5.69 5.39	3.90 3.70	5.31 5.01	1.65 1.39	16.24 14.24	3.18 2.92	3.48 2.93	14.22	20.45 20.19	5.18 4.98	0.25	0.51
inches	0.167 0.131	0.085 0.075	0.045 0.035	0.006 0.004	0.224 0.217	0.224 0.212	0.154 0.146	0.209 0.197	0.065 0.055	0.639 0.560	0.125 0.115	0.137 0.115	0.600	0.805 0.795	0.204 0.196	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT440A						99-03-29

Studless ceramic package; 4 leads SOT441A



DIMENSIONS (mm are the original dimensions)

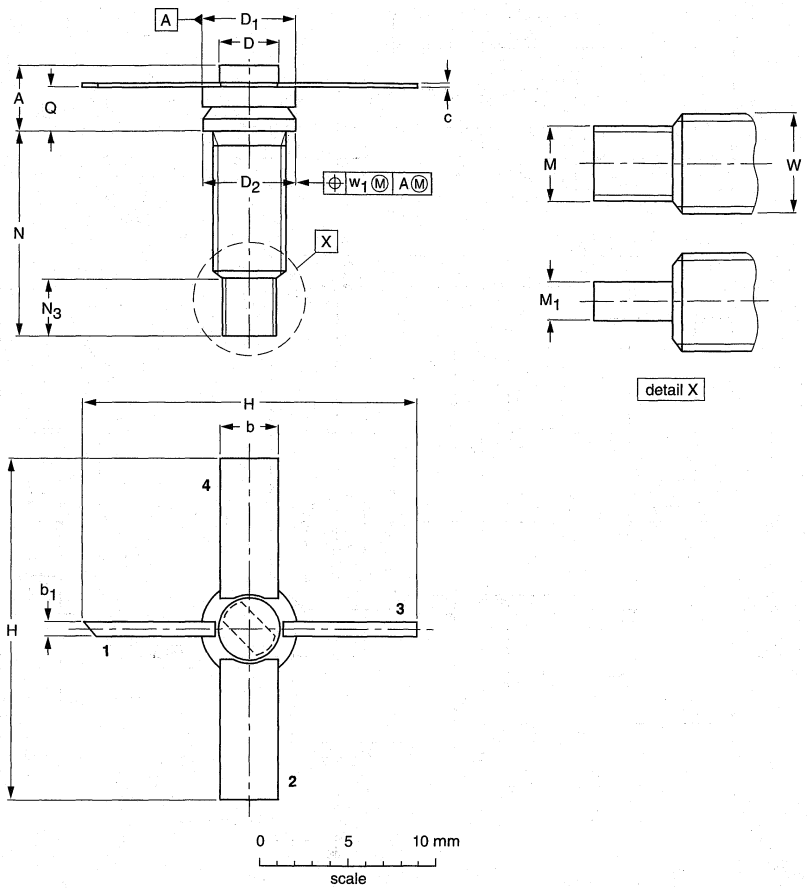
UNIT	A	b	b_1	c	D	D_1	H	Q
mm	2.48 1.60	3.23 3.13	0.81 0.71	0.16 0.10	3.38 3.08	5.34 5.08	19 17	1.15 0.89
inches	0.098 0.063	0.127 0.123	0.032 0.028	0.006 0.004	0.133 0.121	0.210 0.200	0.75 0.67	0.045 0.035

Note

1. This device contains bare beryllium oxide, the dust of witch is toxic.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT441A						99-03-29

Studded ceramic package; 4 leads **SOT442A**



DIMENSIONS (mm are the original dimensions)

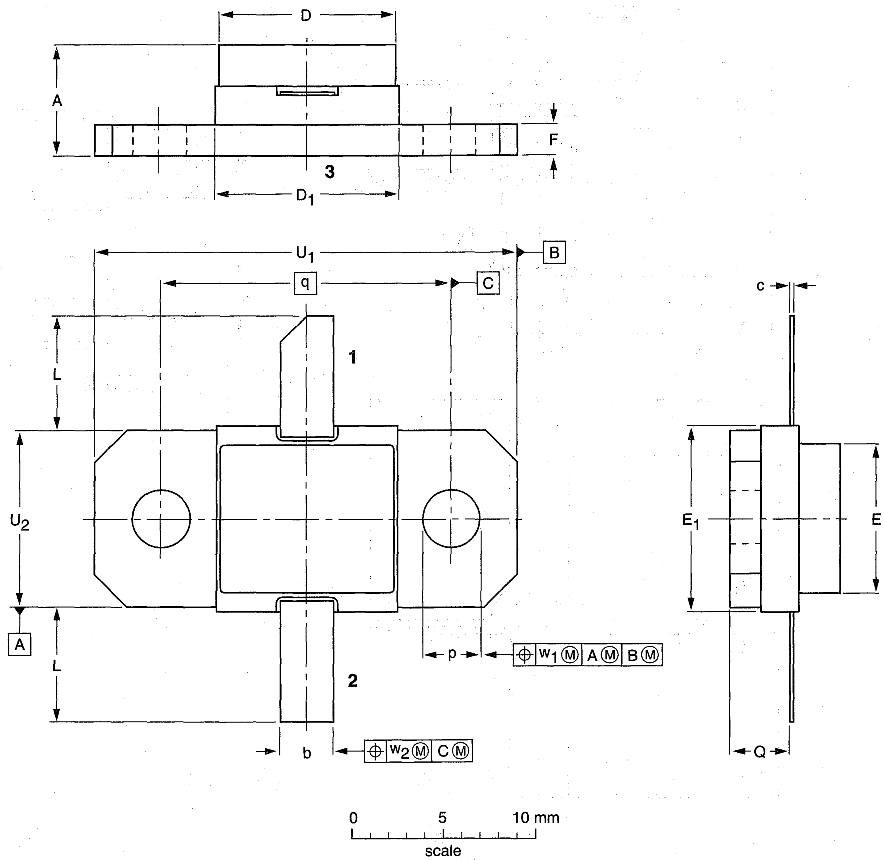
UNIT	A	b	b_1	c	D	D_1	D_2	H	M	M_1	N	N_3	Q	W	w_1
mm	4.05 3.07	3.23 3.13	0.81 0.71	0.16 0.10	3.38 3.08	5.28 5.12	5.23 5.13	19 17	3.05 2.79	1.63 1.42	11.92 10.70	3.68 2.92	2.72 2.36	8-32 UNC	0.38
inches	0.159 0.121	0.127 0.123	0.032 0.028	0.006 0.004	0.133 0.121	0.208 0.202	0.206 0.202	0.75 0.67	0.120 0.110	0.064 0.056	0.470 0.421	0.145 0.115	0.107 0.093		0.015

Note

1. This device contains bare beryllium oxide, the dust of witch is toxic.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT442A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT443A**

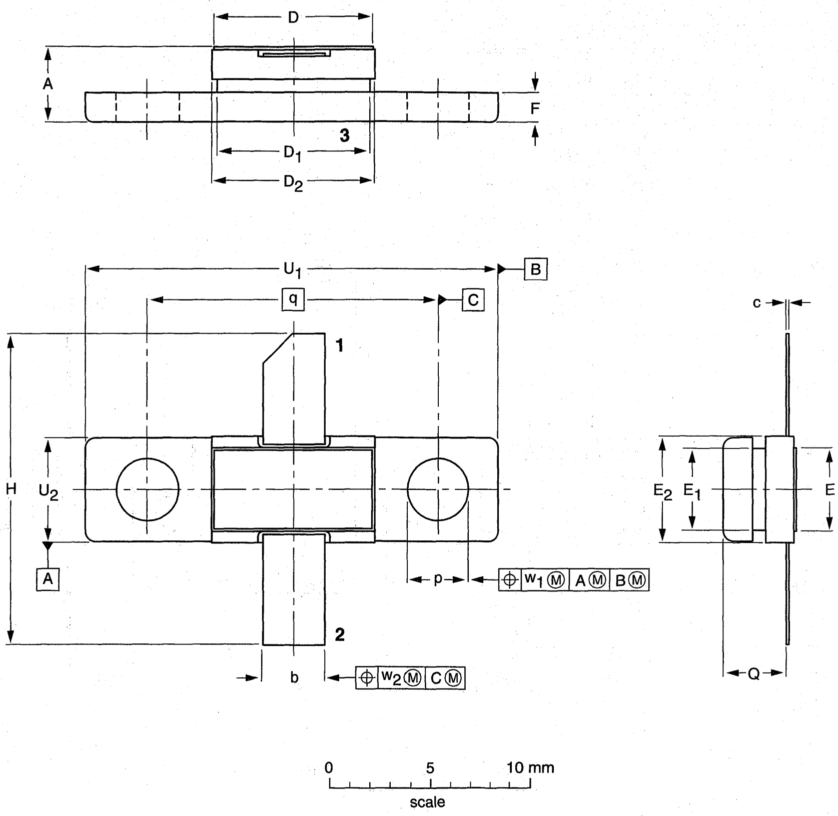


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	6.32 4.90	3.20 2.90	0.15 0.09	10.00 9.70	10.21 9.91	8.15 7.85	10.21 9.91	1.60 1.40	6.25 5.75	3.40 3.20	3.66 2.84	16.50	23.10 22.70	9.90 9.70	0.41	0.94
inches	0.249 0.193	0.126 0.114	0.006 0.004	0.394 0.382	0.402 0.390	0.321 0.309	0.402 0.390	0.063 0.055	0.246 0.226	0.134 0.126	0.144 0.112	0.650	0.909 0.894	0.390 0.382	0.016	0.037

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT443A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT445A**

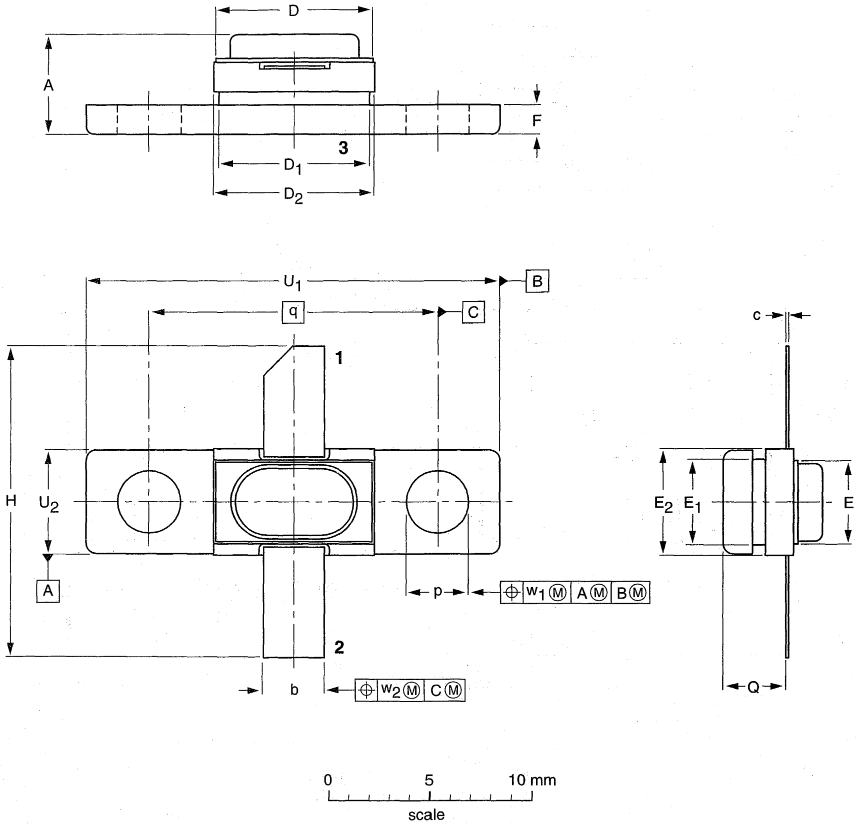


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.01 3.36	3.15 2.95	0.15 0.09	7.9 7.7	7.65 7.35	8.15 7.85	4.1 3.9	4.25 3.95	5.31 5.01	1.67 1.37	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.30	0.51
inches	0.158 0.132	0.125 0.115	0.006 0.003	0.312 0.303	0.302 0.289	0.321 0.309	0.162 0.153	0.168 0.155	0.210 0.197	0.066 0.054	0.624 0.576	0.132 0.120	0.132 0.119	0.56	0.806 0.794	0.204 0.196	0.012	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445A						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT445B**

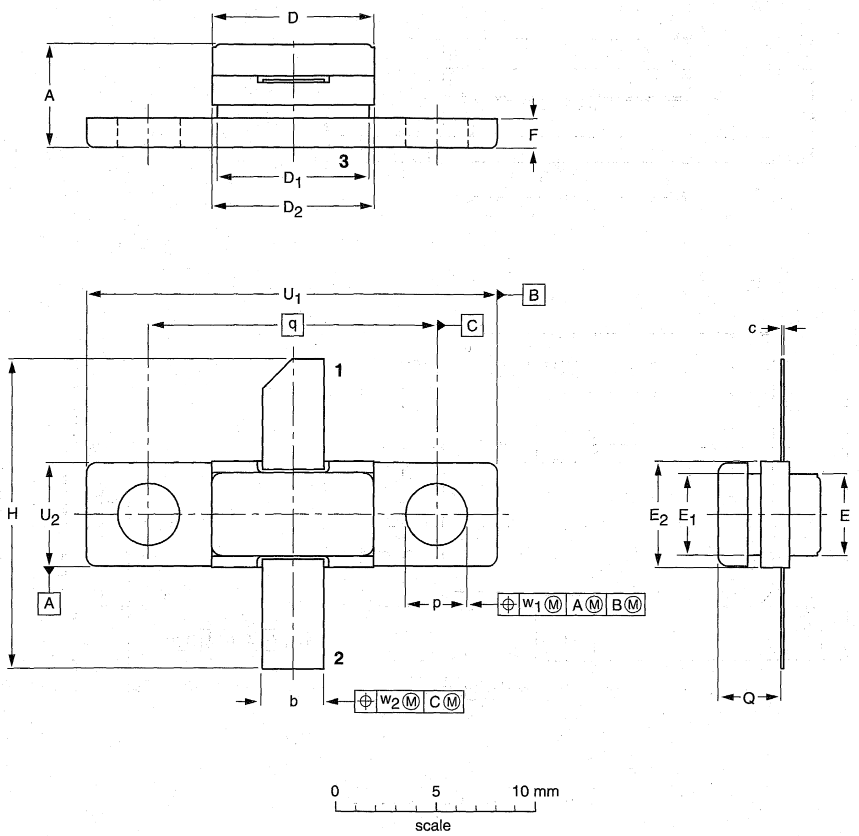


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.27 4.50	3.15 2.95	0.15 0.09	7.85 7.74	7.65 7.35	8.15 7.85	3.97 3.86	4.25 3.95	5.31 5.01	1.67 1.37	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.30	0.51
inches	0.208 0.177	0.125 0.115	0.006 0.003	0.309 0.305	0.302 0.289	0.321 0.309	0.156 0.152	0.168 0.155	0.210 0.197	0.066 0.054	0.624 0.576	0.132 0.120	0.132 0.119	0.56	0.806 0.794	0.204 0.196	0.012	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445B						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT445C**

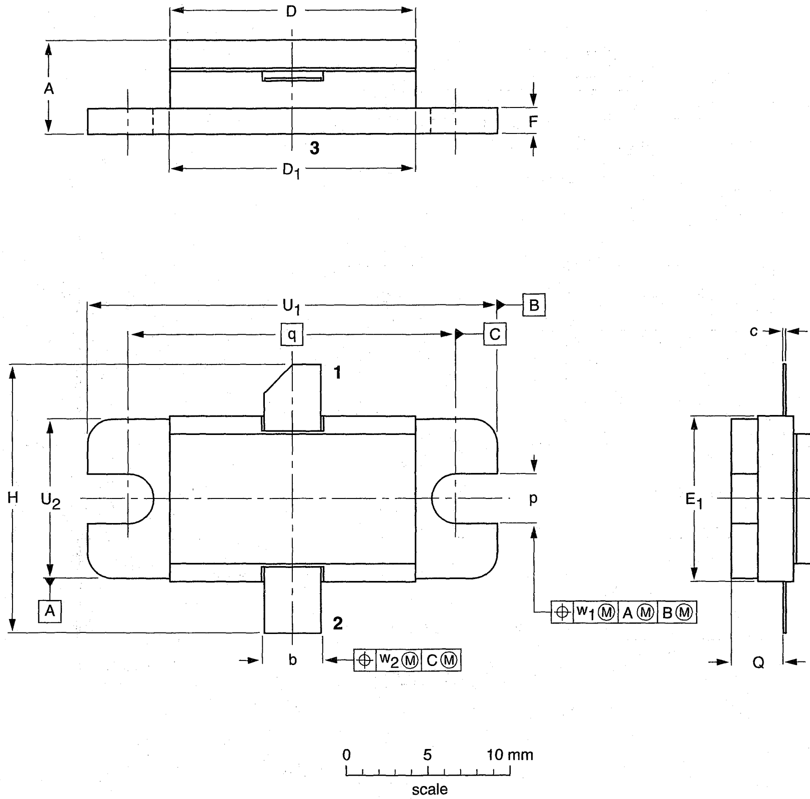


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.57 4.70	3.15 2.95	0.15 0.09	8.13 7.87	7.65 7.35	8.15 7.85	4.20 3.93	4.25 3.95	5.31 5.01	1.67 1.37	15.84 14.64	3.35 3.05	3.33 3.03	14.22	20.47 20.17	5.18 4.98	0.31	0.51
inches	0.220 0.185	0.125 0.115	0.006 0.003	0.32 0.31	0.302 0.289	0.321 0.309	0.165 0.155	0.168 0.155	0.210 0.197	0.066 0.054	0.624 0.576	0.132 0.120	0.132 0.119	0.56	0.806 0.794	0.204 0.196	0.012	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT445C						99-03-29

Flanged hermetic ceramic package; 2 mounting holes; 2 leads **SOT448A**

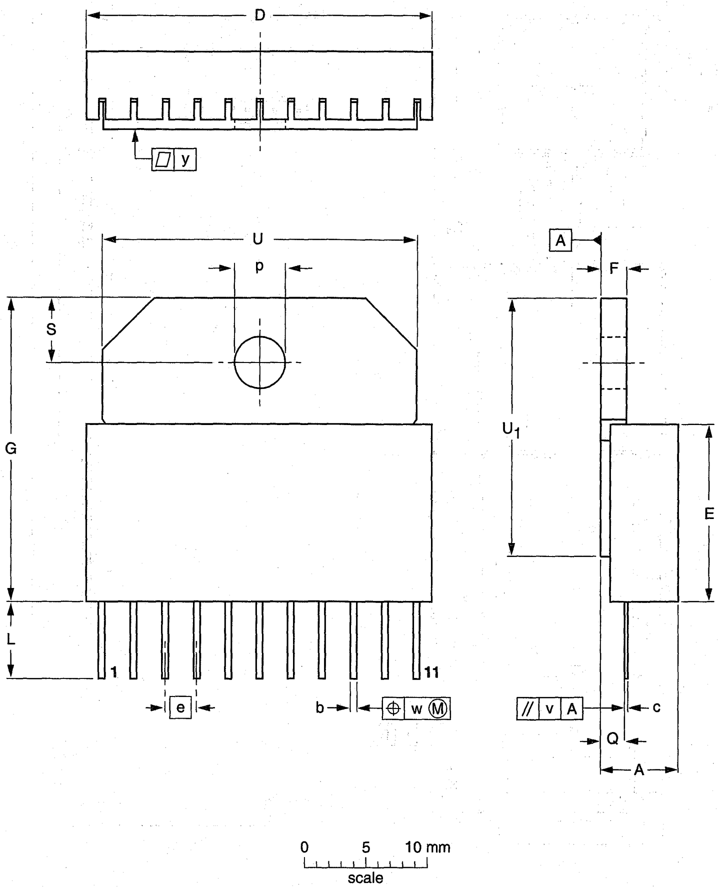


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	6.17 5.31	3.69 3.42	0.13 0.05	15.68 15.16	15.42 15.16	8.08 7.82	10.29 10.03	1.63 1.52	17.02 16.00	3.31 2.79	3.42 3.00	20.32	25.53 25.27	9.91 9.65	0.25	0.79
inches	0.243 0.209	0.145 0.135	0.005 0.002	0.605 0.599	0.607 0.597	0.316 0.310	0.405 0.395	0.064 0.060	0.67 0.63	0.065 0.055	0.134 0.118	0.800	1.005 0.995	0.390 0.380	0.010	0.031

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT448A						99-03-29

Ceramic single-ended flat package; heatsink mounted; 1 mounting hole; 11 in-line gold-metallized leads **SOT451A**



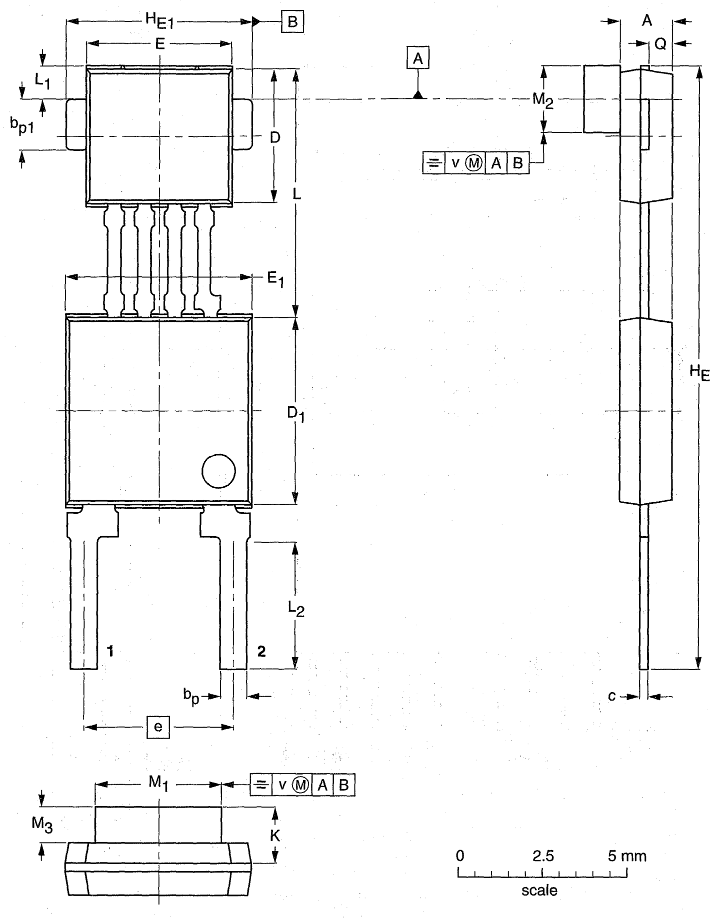
DIMENSIONS (mm are the original dimensions)

UNIT	A	b	c	D	E	e	F	G	L	p	Q	S	U	U_1	v	w	y
mm	5.9 5.5	0.56 0.46	0.25	28.3 27.9	13.9 13.5	2.54	2.2 1.8	23.8 23.4	6.2 5.8	4.2 3.8	2.0 1.6	5.2 4.8	25.4 25.0	20.4 20.0	0.3	0.25	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT451A						97-06-26

Package outlines Chapter 2

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (3.8 x 2 x 0.8 mm); 2 in-line leads **SOT453A**

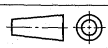


DIMENSIONS (mm are the original dimensions)

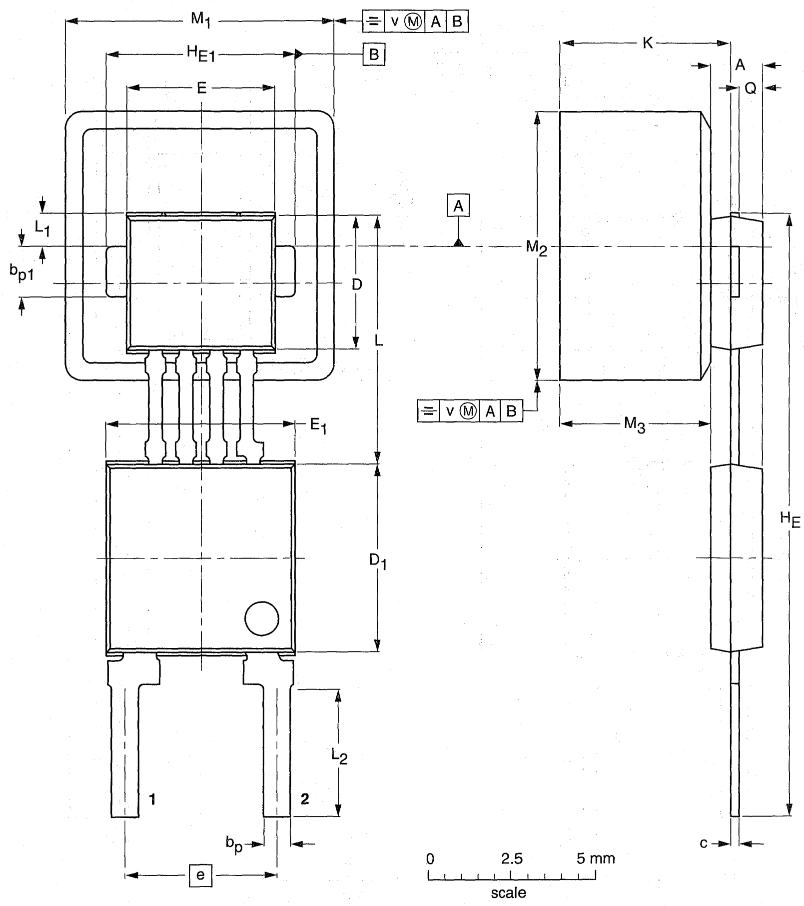
UNIT	A	b_p	b_{p1}	c	D(1)	D_1(1)	E(1)	E_1(1)	e	H_E	H_{E1}	K max.	L	L_1	L_2	M_1	M_2	M_3	Q	v
mm	1.7 1.4	0.8 0.7	1.5 1.4	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	18.2 17.8	5.6 5.5	1.67	7.55 7.25	1.2 0.9	3.9 3.5	3.9 3.7	2.1 1.9	0.9 0.75	0.75 0.65	0.25

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT453A						~~97-02-28~~ 98-03-26

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8 x 8 x 4.5 mm); 2 in-line leads **SOT453B**



DIMENSIONS (mm are the original dimensions)

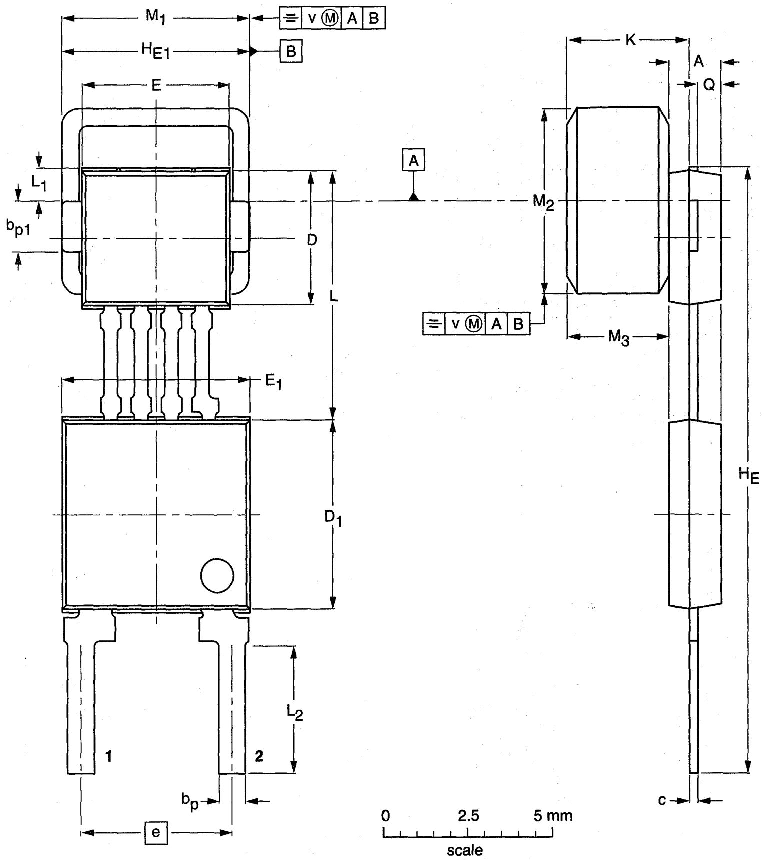
UNIT	A	b_p	b_{p1}	c	D[1]	D_1[1]	E[1]	E_1[1]	e	H_E	H_{E1}	K max.	L	L_1	L_2	M_1	M_2	M_3	Q	v
mm	1.7 1.4	0.8 0.7	1.5 1.4	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	18.2 17.8	5.6 5.5	5.37	7.55 7.25	1.2 0.9	3.9 3.5	8.15 7.85	8.15 7.85	4.7 4.3	0.75 0.65	0.25

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT453B						~~97-02-28~~ 98-03-26

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (5.5 x 5.5 x 3 mm); 2 in-line leads **SOT453C**

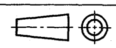


DIMENSIONS (mm are the original dimensions)

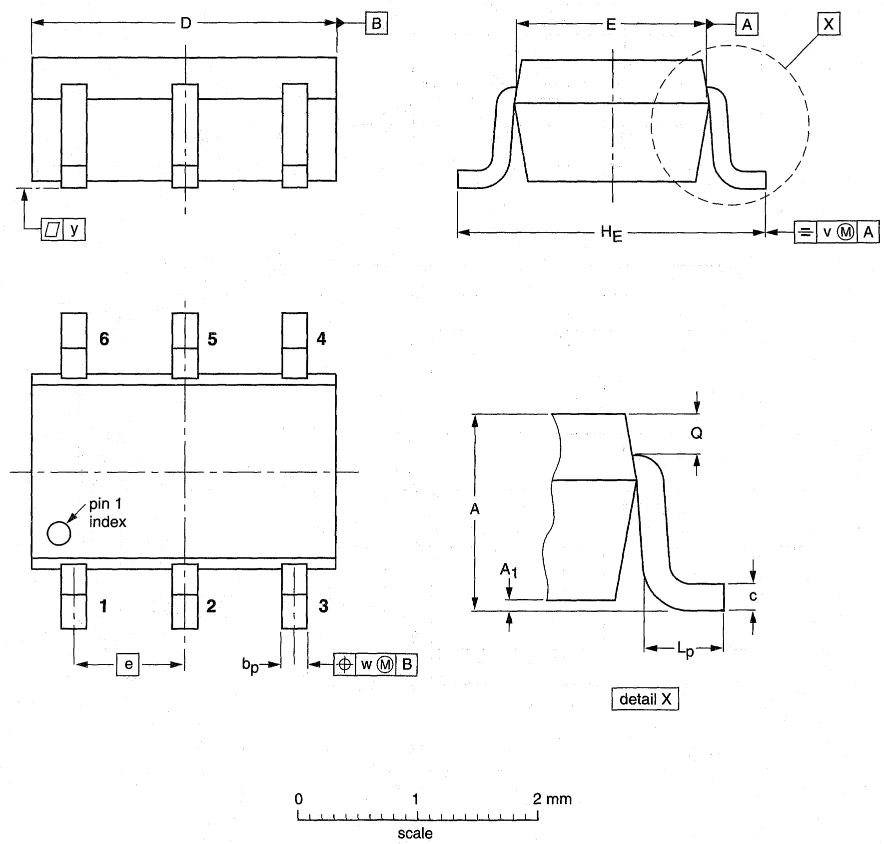
UNIT	A	b_p	b_{p1}	c	$D^{(1)}$	$D_1^{(1)}$	$E^{(1)}$	$E_1^{(1)}$	e	H_E	H_{E1}	K max.	L	L_1	L_2	M_1	M_2	M_3	Q	v
mm	1.7 1.4	0.8 0.7	1.5 1.4	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	18.2 17.8	5.6 5.5	3.87	7.55 7.25	1.2 0.9	3.9 3.5	5.65 5.35	5.65 5.35	3.15 2.85	0.75 0.65	0.25

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT453C						~~97-02-28~~ 98-03-26

Plastic surface mounted package; 6 leads **SOT457**



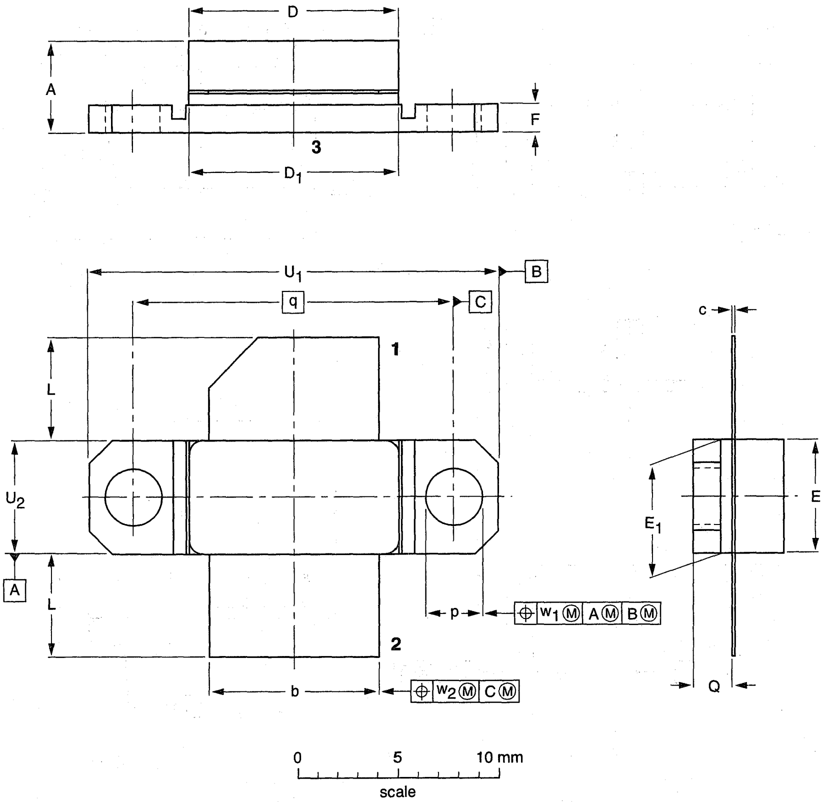
DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b_p	c	D	E	e	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1 0.013	0.40 0.25	0.26 0.10	3.1 2.7	1.7 1.3	0.95	3.0 2.5	0.6 0.2	0.33 0.23	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT457			SC-74			97-02-28

Flanged ceramic package; 2 mounting holes; 2 leads

SOT460A



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

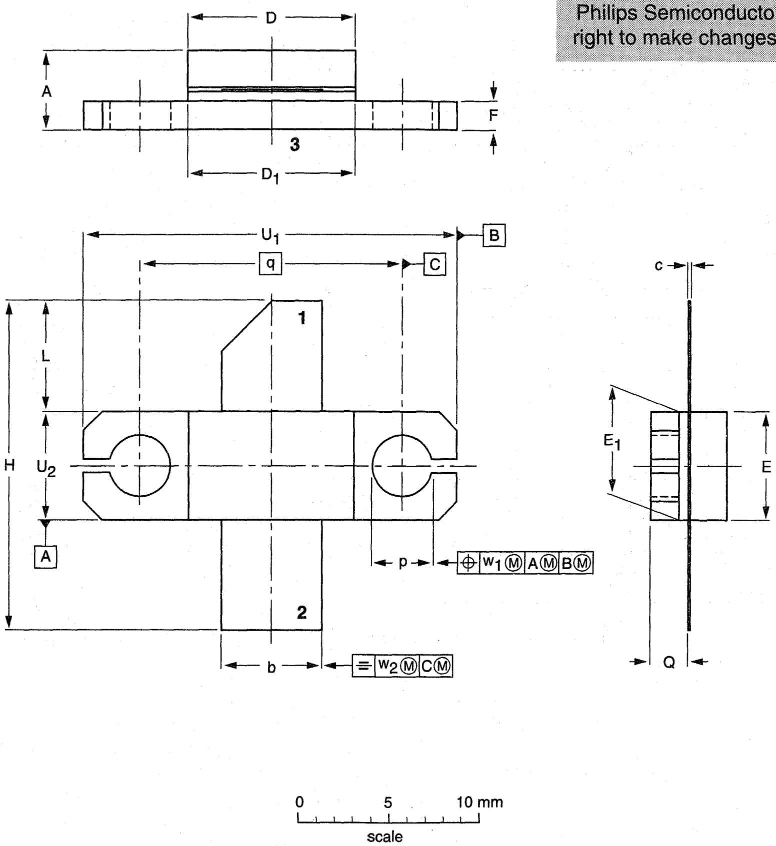
UNIT	A	b	c	D	D_1	E	E_1	F	L	p	Q	q	U_1	U_2	w_1	w_2
mm	5.39 4.49	9.78 9.52	0.16 0.07	12.45 11.68	12.45 11.68	6.94 6.22	6.43 6.17	1.66 1.39	6.10 5.33	3.28 3.02	2.37 1.95	17.98	22.99 22.73	6.43 6.17	0.25	0.51
inches	0.198 0.166	0.385 0.375	0.006 0.003	0.470 0.460	0.470 0.460	0.251 0.245	0.253 0.243	0.065 0.055	0.24 0.21	0.129 0.119	0.093 0.077	0.708	0.905 0.895	0.253 0.243	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT460A						99-03-29

Flanged LDMOST package; 2 mounting holes; 2 leads SOT467A

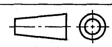
Package under development

Philips Semiconductors reserves the right to make changes without notice.

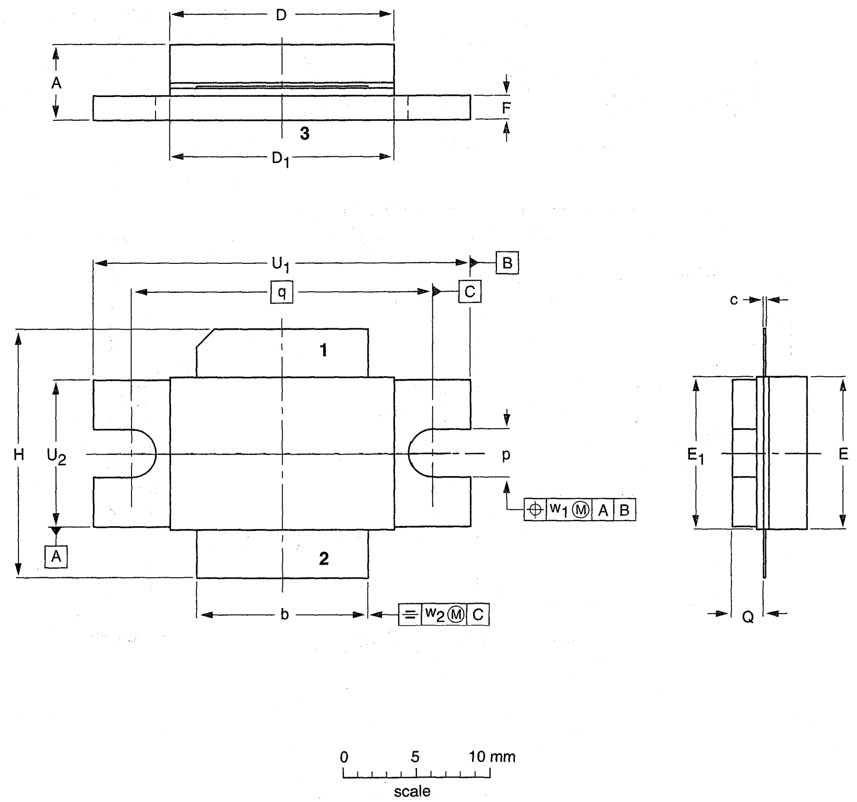


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.29 17.27	6.22 5.71	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.72 0.68	0.135 0.125	0.245 0.225	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467A						99-03-31

Flanged ceramic (AlN) package; 2 mounting holes; 2 leads **SOT468A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

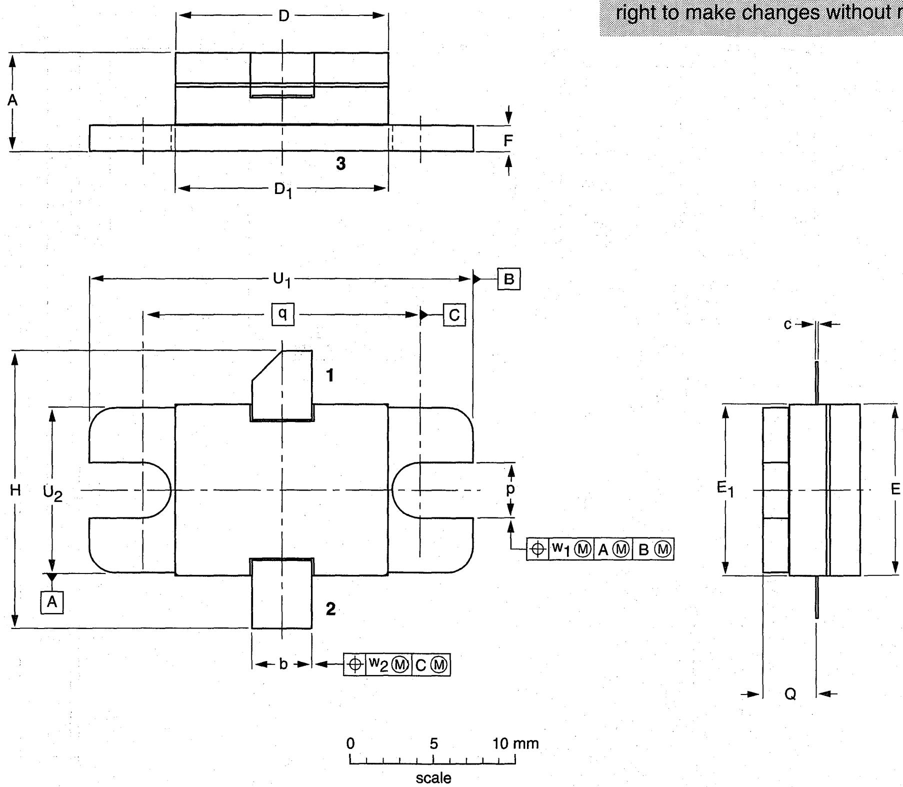
UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.23 4.62	11.81 11.58	0.15 0.10	15.39 15,09	15.37 15,11	10.26 10.06	10.29 10.03	1.65 1.60	16.74 16.48	3.30 3.05	2.21 2.06	20.32	25.53 25.27	9.91 9.65	0.254	0.508
inches	0.206 0.182	0.465 0.455	0.006 0.004	0.606 0.594	0.605 0.595	0.404 0.396	0.405 0.395	0.065 0.063	0.659 0.649	0.130 0.120	0.087 0.081	0.800	1.005 0.995	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT468A						97-12-24

Flanged ceramic package; 2 mounting holes; 2 leads **SOT473A**

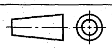
Package under development

Philips Semiconductors reserves the right to make changes without notice.

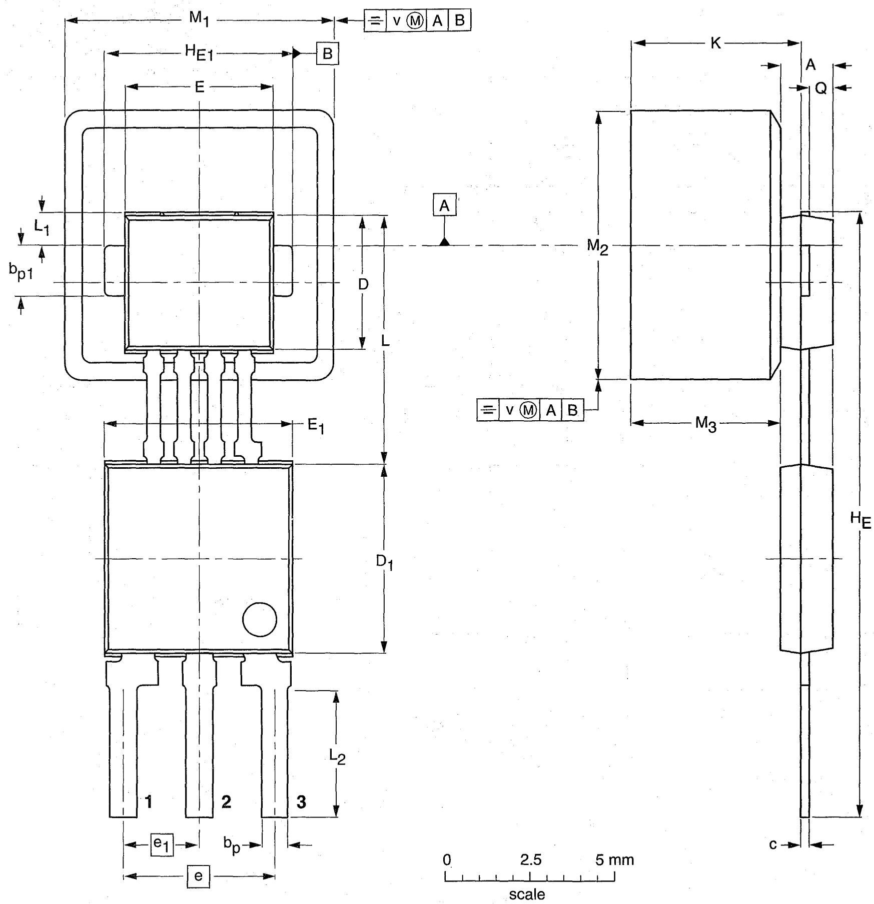


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	6.25 5.18	3.68 3.43	0.13 0.05	12.85 12.55	12.83 12.57	10.31 10.01	10.29 10.03	1.57 1.47	17.27 15.75	3.43 3.18	3.33 2.97	16.51	22.99 22.73	9.91 9.65	0.25	0.51
inches	0.246 0.204	0.145 0.135	0.005 0.002	0.506 0.494	0.505 0.495	0.406 0.396	0.405 0.395	0.062 0.058	0.680 0.620	0.135 0.125	0.131 0.117	0.650	0.905 0.895	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT473A						99-03-31

Plastic single-ended combined package; magnetoresistive sensor element; bipolar IC; magnetized ferrite magnet (8 x 8 x 4.5 mm); 3 in-line leads **SOT477B**



DIMENSIONS (mm are the original dimensions)

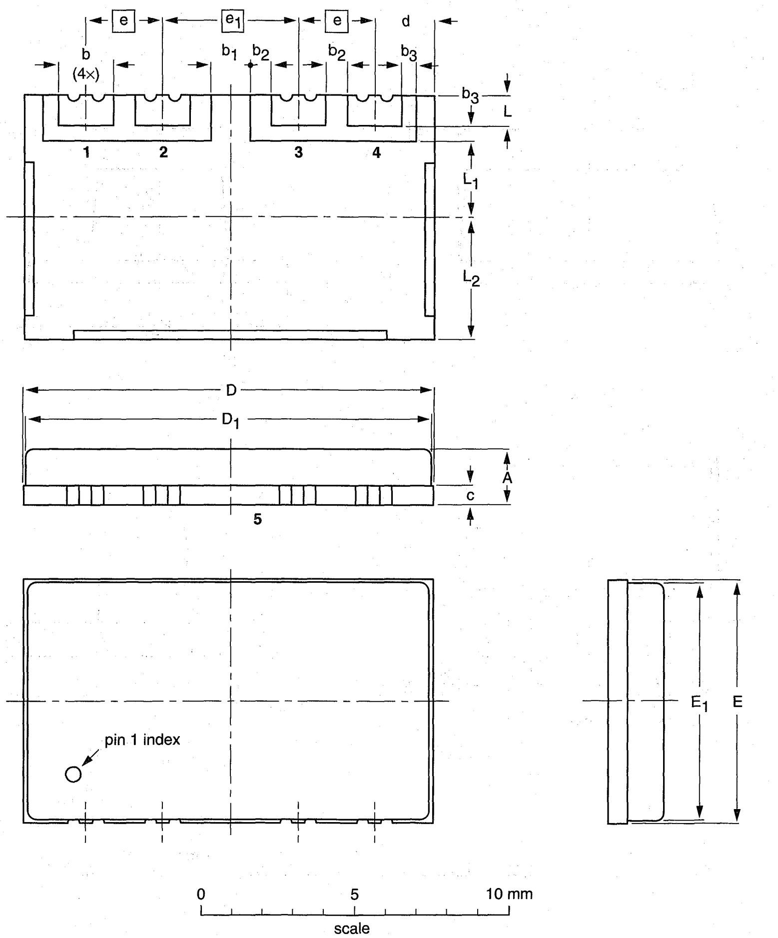
UNIT	A	b_p	b_{p1}	c	D(1)	D_1(1)	E(1)	E_1(1)	e	e_1	H_E	H_{E1}	K max.	L	L_1	L_2	M_1	M_2	M_3	Q	v
mm	1.7 1.4	0.8 0.7	1.57 1.47	0.3 0.24	4.1 3.9	5.7 5.5	4.5 4.3	5.7 5.5	4.6 4.4	2.35 2.15	18.2 17.8	5.6 5.5	5.37	7.55 7.25	1.2 0.9	3.9 3.5	8.15 7.85	8.15 7.85	4.7 4.3	0.75 0.65	0.25

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT477B						99-02-16

Leadless surface mounted package; plastic cap; 4 terminations **SOT482B**

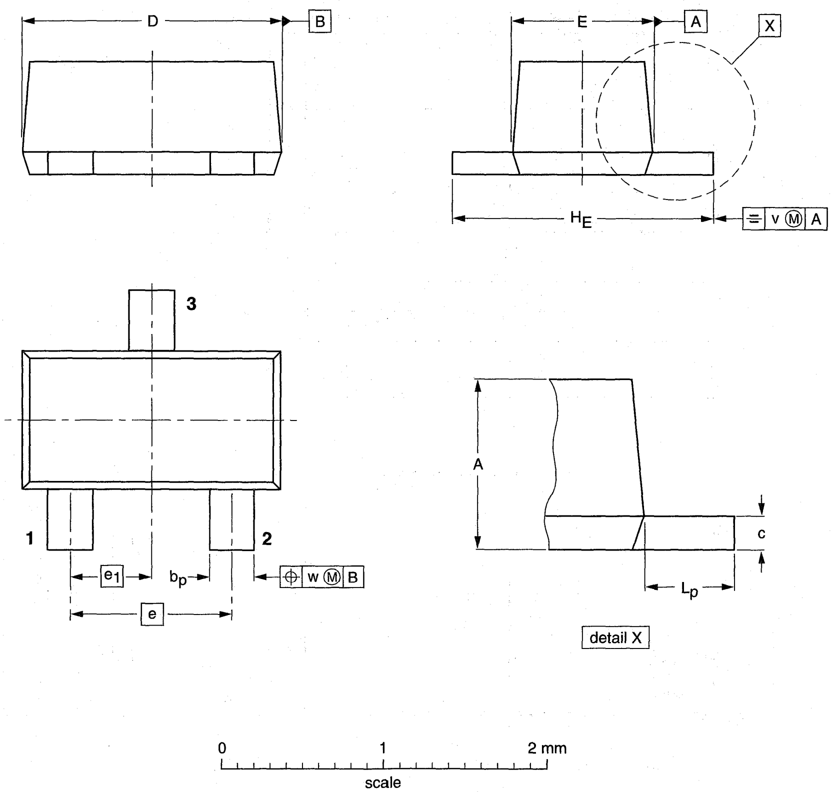


DIMENSIONS (mm are the original dimensions)

UNIT	A	b	b_1	b_2	b_3	c	D	D_1	d	E	E_1	e	e_1	L	L_1	L_2
mm	2.00 1.59	1.9 1.7	1.4 1.2	0.8 0.6	0.6 0.4	0.70 0.57	13.7 13.3	13.35 13.05	2.0	8.2 7.8	7.85 7.55	2.6 2.4	4.6 4.4	1.15 0.85	2.65 2.35	3.85 3.55

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT482B						99-02-05

Plastic surface mounted package; 3 leads **SOT490**



DIMENSIONS (mm are the original dimensions)

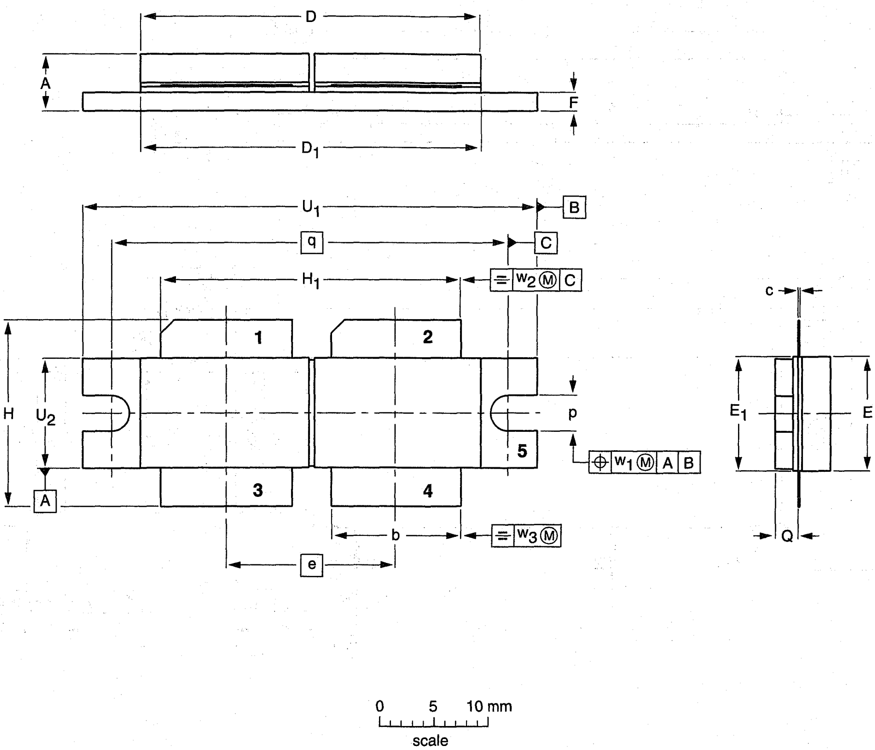
UNIT	A	b_p	c	D	E	e	e_1	H_E	L_p	v	w
mm	0.8 0.6	0.33 0.23	0.2 0.1	1.7 1.5	0.95 0.75	1.0	0.5	1.7 1.5	0.5 0.3	0.1	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT490			SC-89			98-10-23

Flanged double-ended ceramic (AlN) package; 2 mounting holes; 4 leads **SOT494A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.

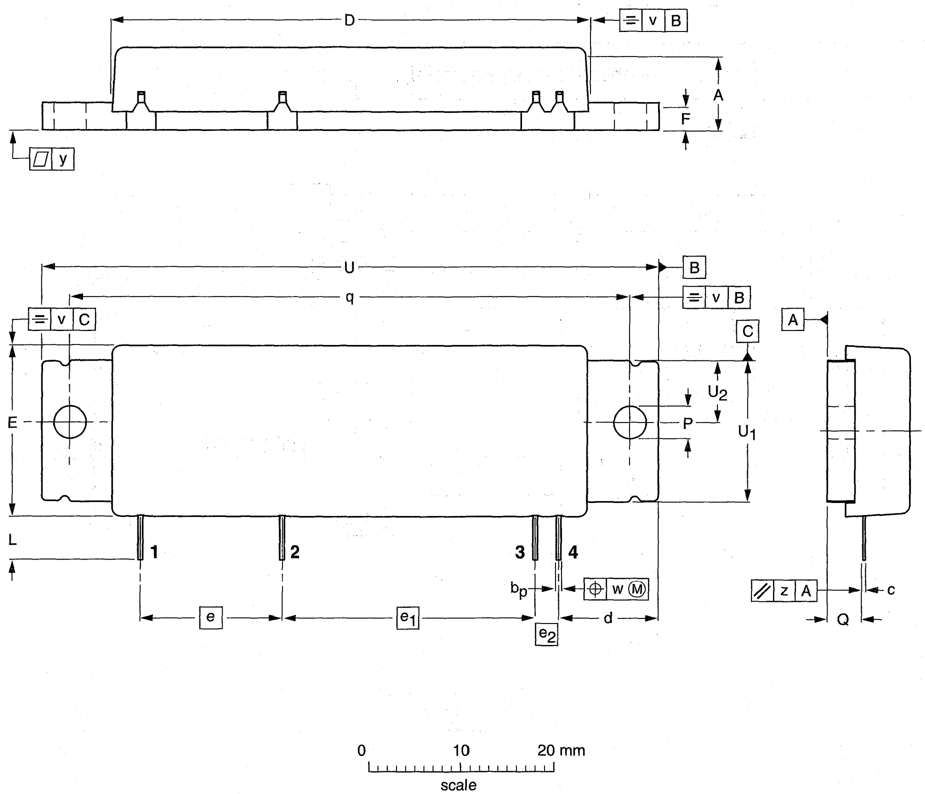


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	e	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.26 4.60	11.81 11.56	0.15 0.10	33.96 28.02	31.37 30.61	10.26 10.06	10.29 10.03	15.75	1.66 1.60	16.74 16.48	27.81 27.05	3.30 3.05	2.21 2.06	36.07	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.207 0.181	0.465 0.455	0.006 0.004	1.337 1.103	1.235 1.205	0.404 0.396	0.405 0.395	0.62	0.065 0.063	0.659 0.649	1.095 1.065	0.130 0.120	0.087 0.081	1.42	1.625 1.615	0.405 0.395	0.01	0.02	0.01

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT494A						99-03-30

Plastic rectangular single-ended flat package; flange mounted; 2 mounting holes; 4 in-line leads **SOT501A**



DIMENSIONS (mm are the original dimensions)

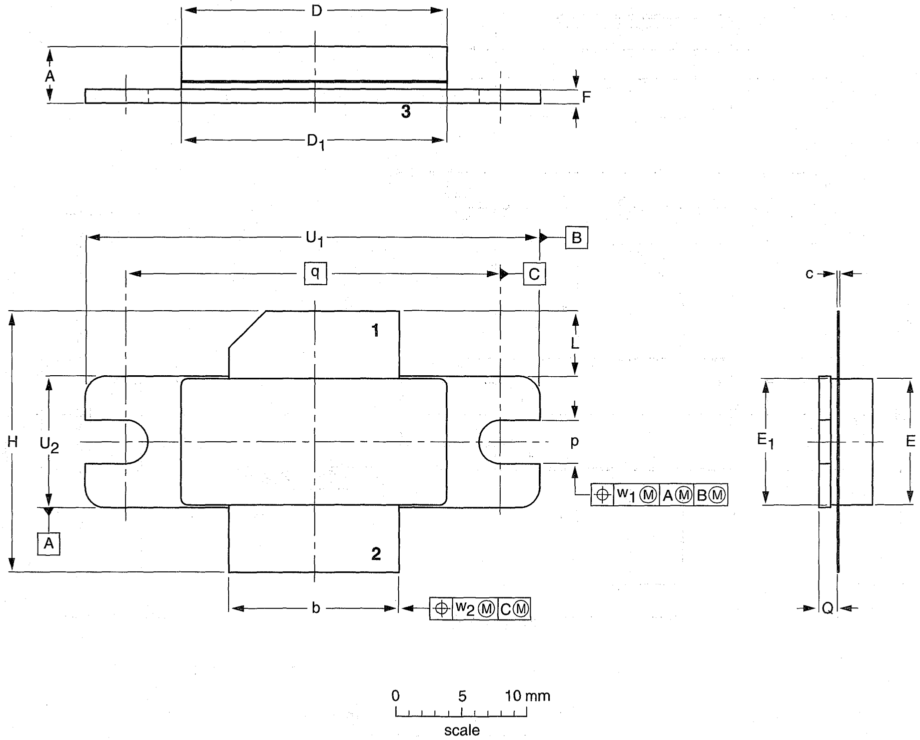
UNIT	A	b_p	c	D	d	E	e	e_1	e_2	F	L	P	Q	q	U	U_1	U_2	v	w	y	z
mm	9.4 8.9	0.56 0.46	0.3 0.2	52.1 51.7	10.9 10.5	18.7 18.3	15.24	27.94	2.54	3.1 2.9	6.5 6.1	3.6 3.4	4.1 3.7	61.2 61.0	67.4 67.0	15.5 15.1	6.9 6.5	0.2	0.25	0.1	0.3

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT501A						98-10-28

Flanged LDMOST package; 2 mounting holes; 2 leads **SOT502A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.

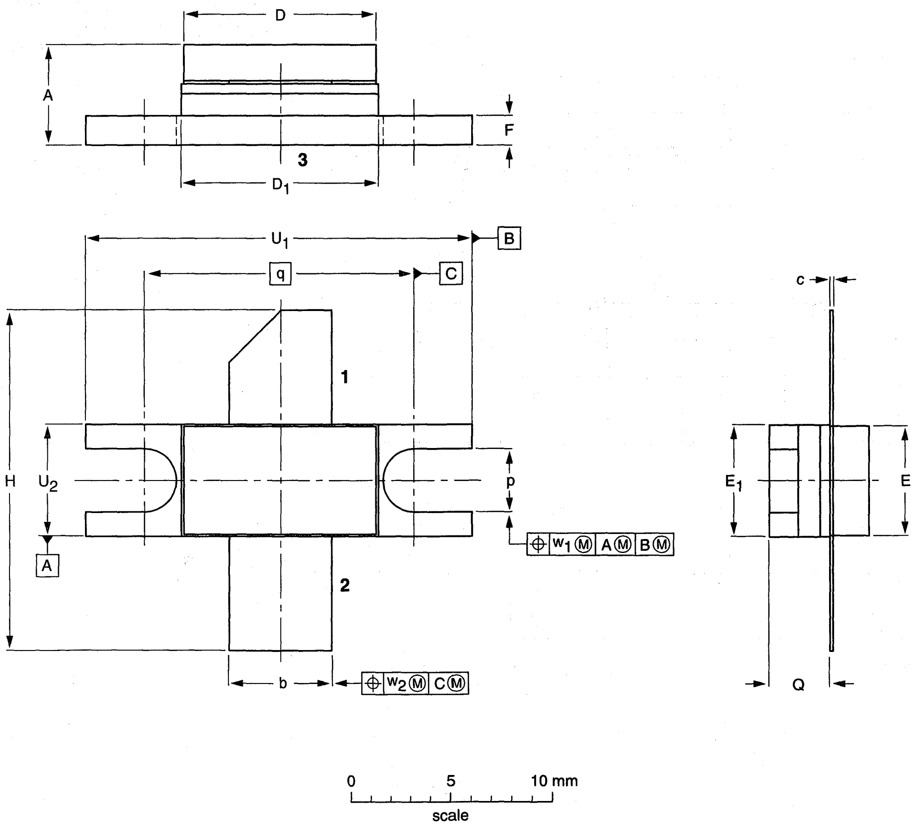


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	L	p	Q	q	U_1	U_2	w_1	w_2
mm	4.72 3.99	12.83 12.57	0.15 0.08	20.02 19.61	19.96 19.66	9.50 9.30	9.50 9.25	1.14 0.89	19.94 18.92	5.33 4.32	3.38 3.12	1.70 1.45	27.94	34.16 33.91	9.91 9.65	0.25	0.51
inches	0.186 0.157	0.505 0.495	0.006 0.003	0.788 0.772	0.786 0.774	0.374 0.366	0.374 0.364	0.045 0.035	0.785 0.745	0.210 0.170	0.133 0.123	0.067 0.057	1.100	1.345 1.335	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT502A						99-03-30

Flanged ceramic package; 2 mounting holes; 2 leads **SOT504A**

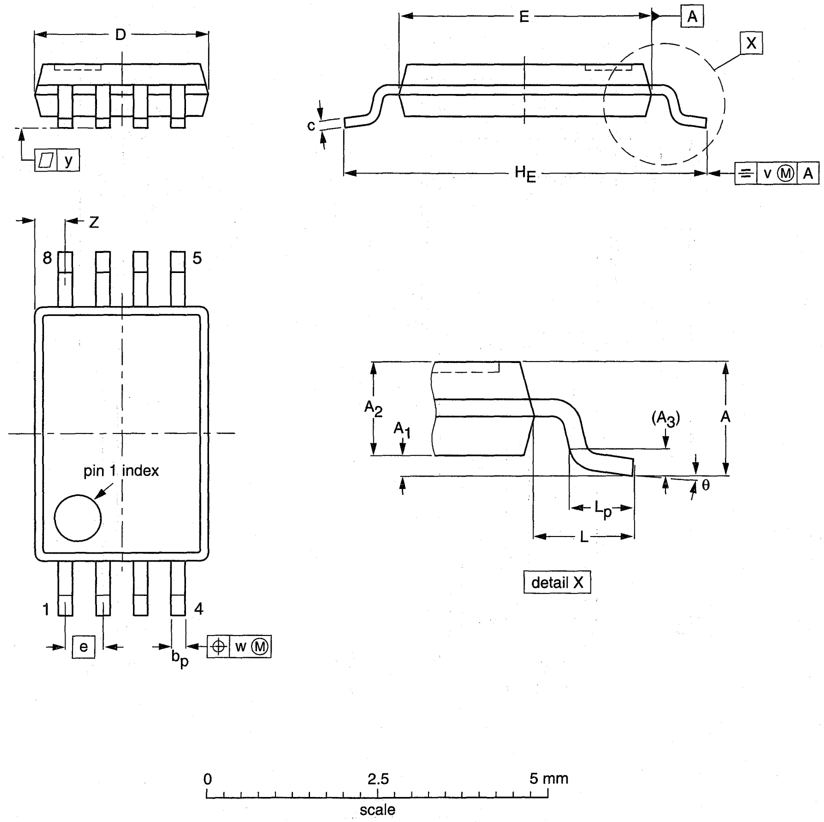


DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.84 4.85	5.59 5.33	0.18 0.10	10.26 10.06	10.54 10.29	5.79 5.64	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	3.43 2.92	14.22	20.45 20.19	5.97 5.72	0.25	0.51
inches	0.230 0.191	0.220 0.210	0.007 0.004	0.404 0.396	0.415 0.405	0.228 0.222	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.135 0.115	0.56	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT504A						99-03-29

TSSOP8: plastic thin shrink small outline package; 8 leads; body width 4.4 mm **SOT530-1**



DIMENSIONS (mm are the original dimensions)

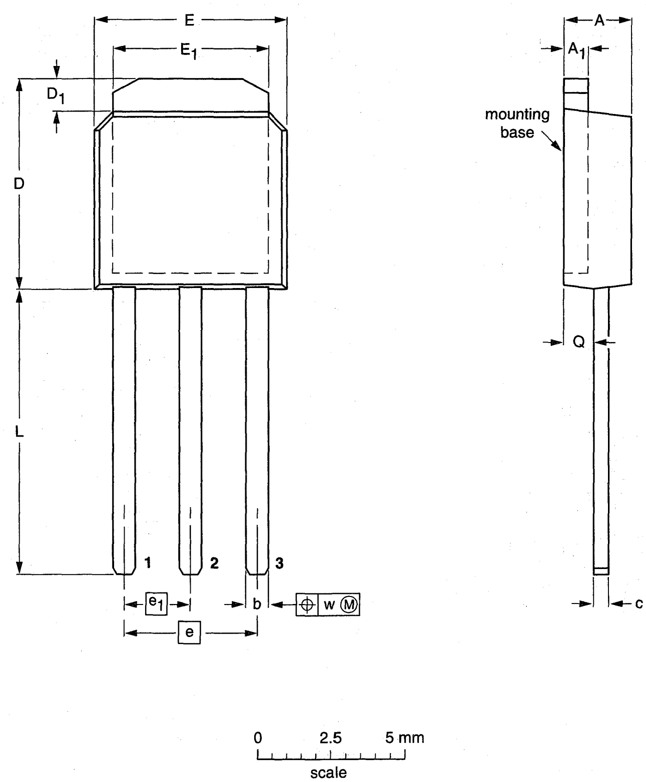
UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(2)}$	e	H_E	L	L_p	v	w	y	$Z^{(1)}$	θ
mm	1.10	0.15 0.05	0.95 0.85	0.65	0.30 0.19	0.20 0.13	3.10 2.90	4.50 4.30	0.65	6.50 6.30	0.94	0.70 0.50	0.10	0.10	0.10	0.70 0.35	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

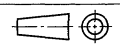
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT530-1		MO-153AA				98-11-25

Plastic single-ended package (Philips version of I-PAK); 3 leads (in-line) **SOT533**



DIMENSIONS (mm are the original dimensions)

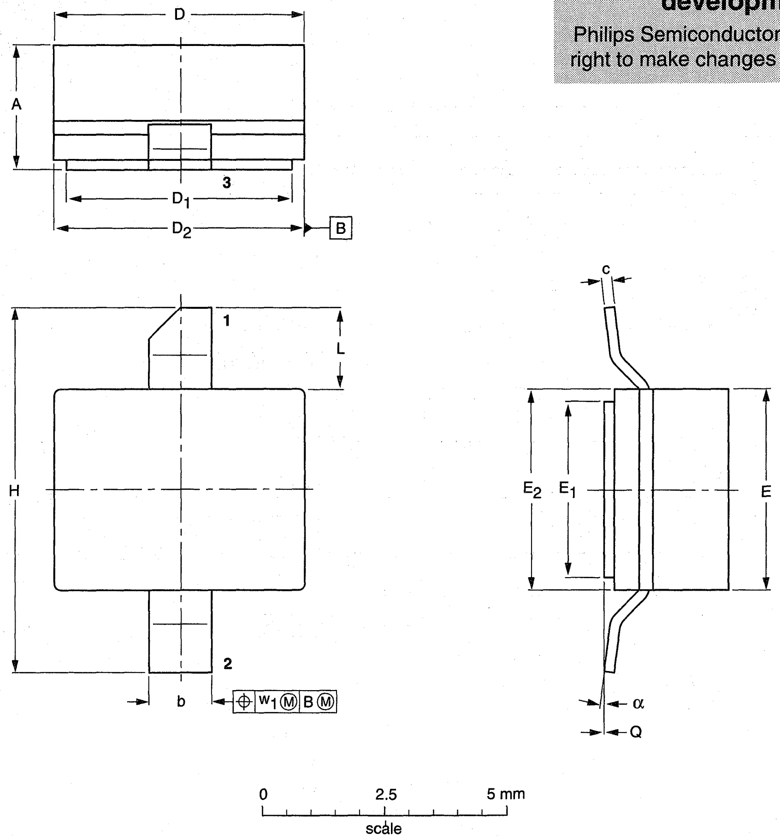
UNIT	A	A_1	b	c	D	D_1	E	E_1	e	e_1	L	Q
mm	2.38 2.22	0.89 0.71	0.89 0.71	0.56 0.46	7.28 6.94	1.06 0.96	6.73 6.47	5.36 5.26	4.57	2.285	9.8 9.4	1.00 1.10

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT533		TO-251				99-02-18

Ceramic surface mounted package; 2 leads **SOT538A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

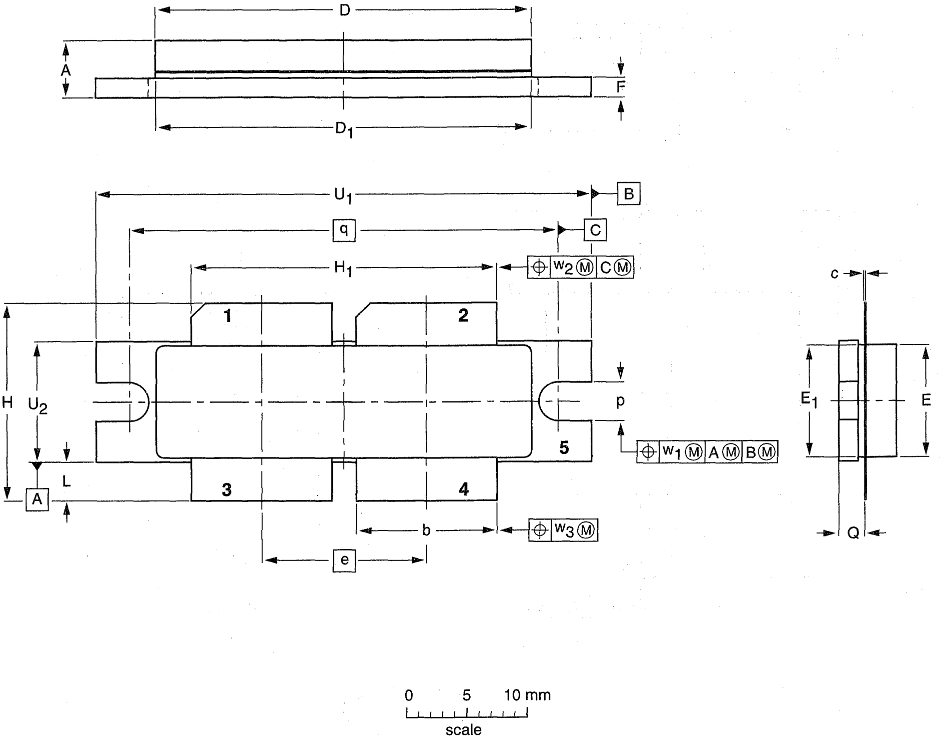
UNIT	A	b	c	D	D_1	D_2	E	E_1	E_2	H	L	Q	w_1	α
mm	2.95 2.29	1.35 1.19	0.23 0.18	5.16 5.00	4.65 4.50	5.41 5.00	4.14 3.99	3.63 3.48	4.14 3.99	7.49 7.24	2.03 1.27	0.10 0.00	0.25	7° 0°
inches	0.116 0.090	0.053 0.047	0.009 0.007	0.203 0.197	0.183 0.177	0.213 0.197	0.163 0.157	0.143 0.137	0.163 0.157	0.295 0.285	0.080 0.050	0.004 0.000	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT538A						99-03-30

Flanged balanced LDMOST package; 2 mounting holes; 4 leads **SOT539A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

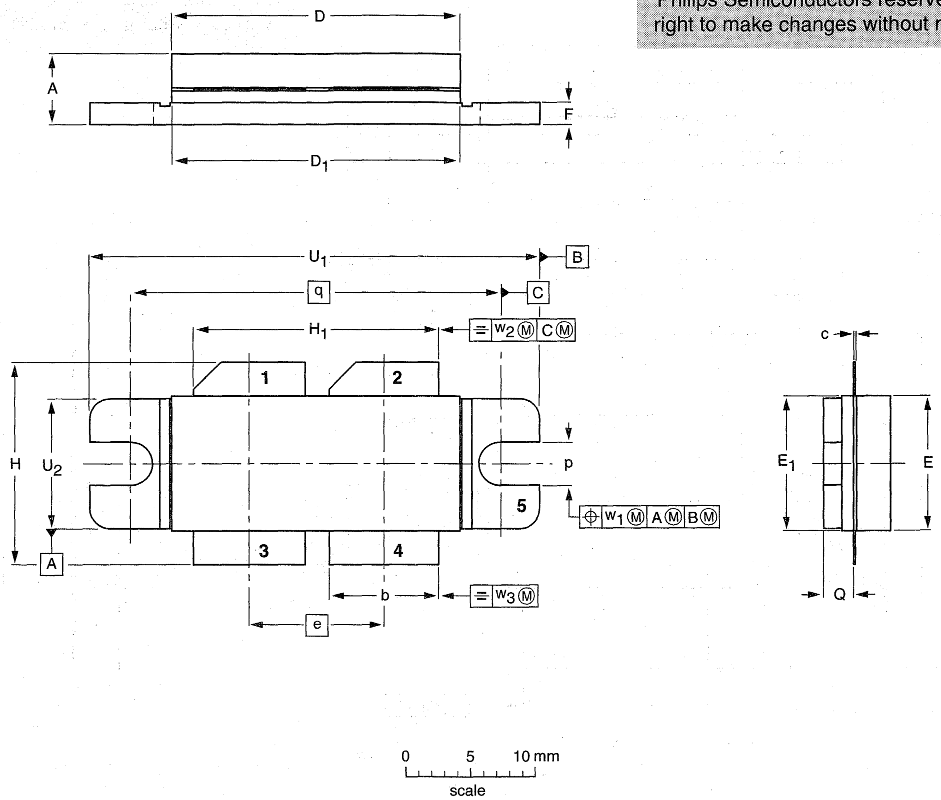
UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	L	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.33 4.55	11.81 11.56	0.15 0.08	31.55 30.94	31.65 30.96	13.72	9.50 9.20	9.53 9.27	1.75 1.50	17.12 16.10	25.53 25.27	3.73 2.72	3.30 3.05	2.31 2.01	35.56	41.28 41.02	10.29 10.03	0.25	0.51	0.25
inches	0.210 0.179	0.465 0.455	0.006 0.003	1.242 1.218	1.246 1.219	0.540	0.374 0.366	0.375 0.365	0.069 0.059	0.674 0.634	1.005 0.995	0.147 0.107	0.130 0.120	0.091 0.079	1.400	1.625 1.615	0.405 0.395	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT539A						99-05-10

Flanged balanced LDMOST package; 2 mounting holes; 4 leads **SOT540A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



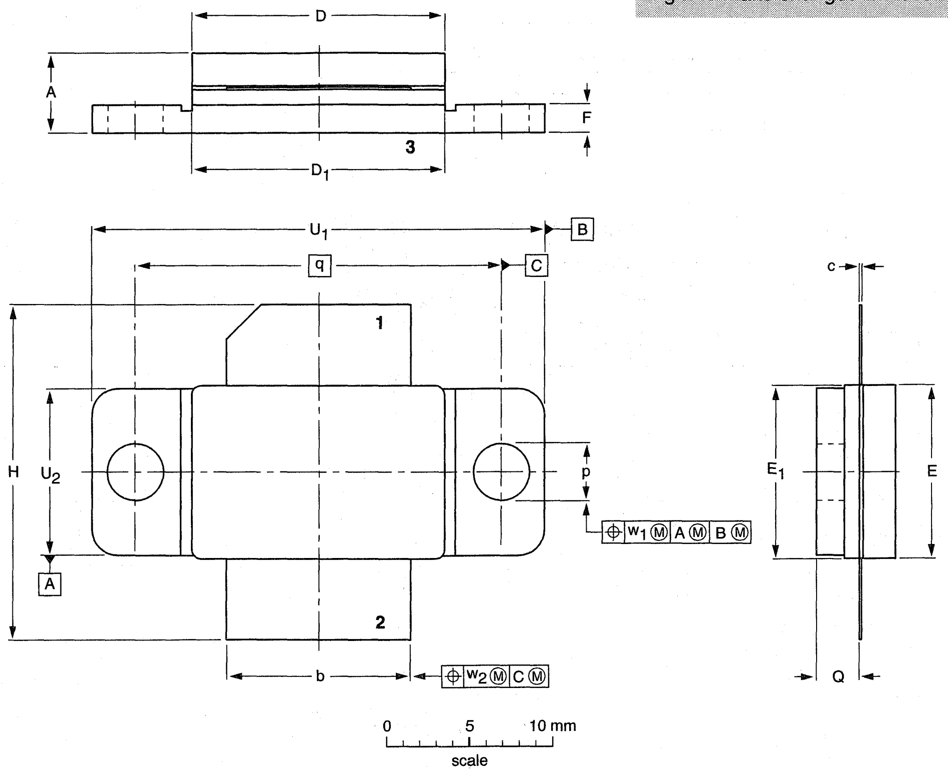
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	e	E	E_1	F	H	H_1	p	Q	q	U_1	U_2	w_1	w_2	w_3
mm	5.77 5.00	8.51 8.26	0.15 0.10	22.05 21.64	22.05 21.64	10.21	10.26 10.06	10.31 10.01	1.78 1.52	15.75 14.73	18.72 18.47	3.38 3.12	2.72 2.46	27.94	34.16 33.91	9.91 9.65	0.25	0.51	0.25
inches	0.227 0.197	0.335 0.325	0.006 0.004	0.868 0.852	0.868 0.852	0.402	0.404 0.396	0.406 0.394	0.070 0.060	0.620 0.580	0.737 0.727	0.133 0.123	0.107 0.097	1.100	1.345 1.335	0.390 0.380	0.010	0.020	0.010

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT540A						99-03-30

Flanged LDMOST package; 2 mounting holes; 2 leads **SOT541A**

Package under development
Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

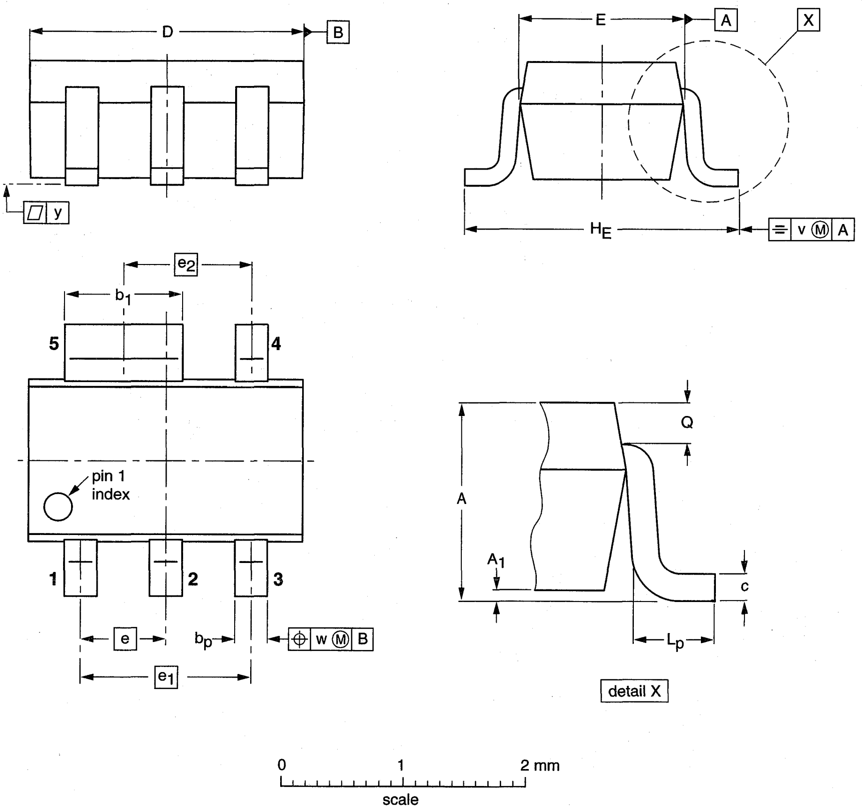
UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.13 4.34	11.05 10.80	0.18 0.10	15.39 15.09	15.39 15.09	10.26 10.06	10.29 10.03	1.78 1.52	20.83 19.81	3.43 3.18	2.69 2.44	22.10	27.31 27.05	9.91 9.65	0.25	0.51
inches	0.202 0.171	0.435 0.425	0.007 0.004	0.606 0.594	0.606 0.594	0.404 0.396	0.405 0.395	0.070 0.060	0.820 0.780	0.135 0.125	0.106 0.096	0.87	1.075 1.065	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT541A						99-04-08

Plastic surface mounted package; 5 leads | **SOT551A**

Package under development

Philips Semiconductors reserves the right to make changes without notice.



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 max	b_p	b_1	c	D	E	e	e_1	e_2	H_E	L_p	Q	v	w	y
mm	1.1 0.9	0.1	0.3 0.2	0.8 1.0	0.25 0.10	2.2 1.8	1.35 1.15	0.65	1.3	0.975	2.2 2.0	0.45 0.15	0.25 0.15	0.2	0.2	0.1

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT551A						1999-05-07

CHAPTER 3

HANDLING PRECAUTIONS

Handling precautions

Chapter 3

ELECTROSTATIC CHARGES

Electrostatic charges can be stored in many things; for example, man-made fibre clothing, moving machinery, objects with air blowing across them, plastic storage bins, sheets of paper stored in plastic envelopes, paper from electrostatic copying machines, and people (see Fig.1). The charges are caused by friction between two surfaces, at least one of which is non-conductive. The magnitude and polarity of the charges depend on the different affinities for electrons of the two materials rubbing together, the friction force and the humidity of surrounding air.

Electrostatic discharge (ESD) is the transfer of an electrostatic charge between bodies at different potentials and occurs with direct contact or when induced by an electrostatic field. All pins of Philips semiconductor devices are protected against electrostatic discharge. However we recommend that the following ESD precautions are complied with when handling such components.

WORKSTATION FOR HANDLING ELECTROSTATIC-SENSITIVE DEVICES

Figure 1 shows a working area suitable for safely handling electrostatic-sensitive devices. It has a workbench, the surface of which is conductive and anti-static. The floor should also be covered with anti-static material.

The following precautions should be observed:

- Persons at a workbench should be earthed via a wrist strap and a resistor.
- All mains-powered equipment should be connected to the mains via an earth-leakage switch.
- Equipment cases should be grounded.
- Relative humidity should be maintained between 40% and 50%.
- An ionizer should be used to neutralize objects with immobile static charges in case other solutions fail.
- Keep static materials, such as plastic envelopes and plastic trays etc., away from the workbench. If there are any such static materials on the workbench, remove them before handling the semiconductor devices.
- Refer to the current version of the handbook EN 100015 (CECC 00015) *"Protection of Electrostatic Sensitive Devices"*, which explains in more detail how to arrange an ESD protective area for handling ESD sensitive devices.

RECEIPT AND STORAGE OF COMPONENTS

Electrostatic-sensitive devices are packed for despatch in anti-static/conductive containers, usually boxes, tubes or blister tape. Warning labels on both primary and secondary packing show that the contents are sensitive to electrostatic discharge.

Such devices should be kept in their original packing whilst in storage. If a bulk container is partially unpacked, the unpacking should be done at a protected workstation. Any components that are stored temporarily should be packed in conductive or anti-static packing or carriers.

PCB ASSEMBLY

Electrostatic-sensitive devices must be removed from their protective packing with grounded component-pincers or short-circuit clips. Short-circuit clips must remain in place during mounting, soldering and cleansing/drying processes. Don't remove more components from the storage packing than are needed at any one time. Production/assembly documents should state that the product contains electrostatic sensitive devices and that special precautions need to be taken. During assembly, ensure that the electrostatic-sensitive devices are the last of the components to be mounted and that this is done at a protected workstation.

All tools used during assembly, including soldering tools and solder baths, must be grounded. All hand-tools should be of conductive or anti-static material and, where possible, should not be insulated.

TESTING PCBs

Completed PCBs must be tested at a protected workstation. Place the soldered side of the circuit board on conductive or anti-static foam and remove the short-circuit clips. Remove the circuit board from the foam, holding the board only at the edges. Make sure the circuit board doesn't touch the conductive surface of the workbench. After testing, replace the PCB on the conductive foam to await packing.

Assembled circuit boards containing electrostatic-sensitive devices should always be handled in the same way as unmounted components. They should also carry warning labels and be packed in conductive or anti-static packing.

Handling precautions

Chapter 3

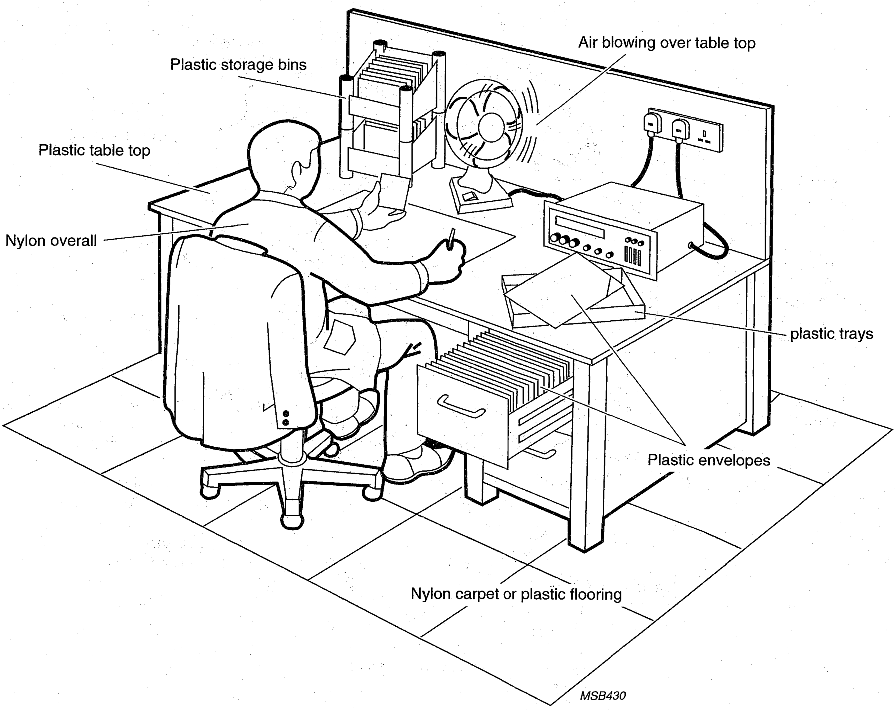


Fig.1 Poor working environment for electronic component handling showing potential ESD hazards.

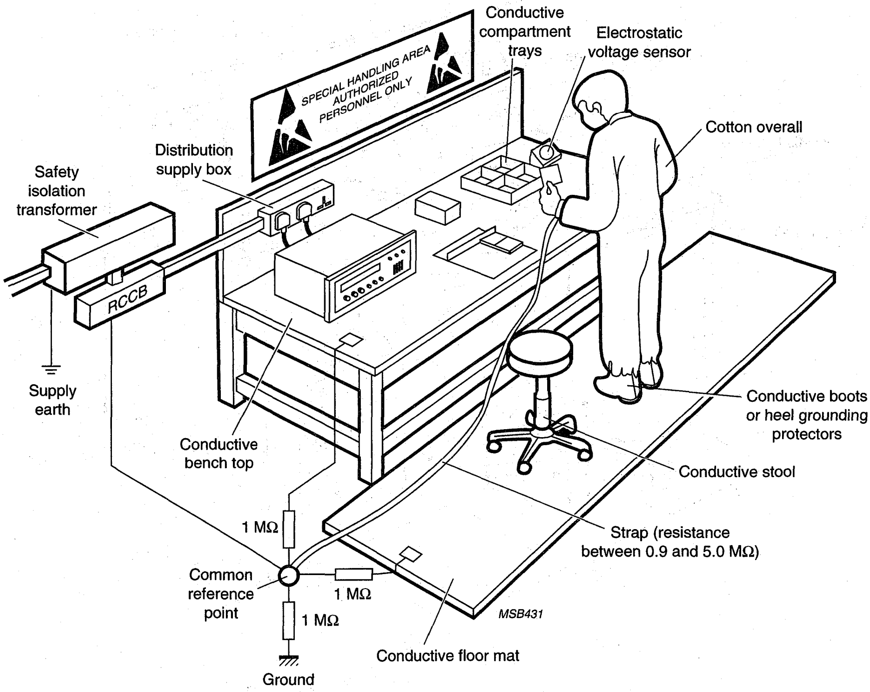


Fig.2 Essential features of an ESD-protected workstation.

CHAPTER 4

SOLDERING GUIDELINES AND SMD FOOTPRINT DESIGN

Soldering guidelines and SMD footprint design

Chapter 4

INTRODUCTION

There are two basic forms of electronic component construction, those with leads for through-hole mounting and microminiature types for surface mounting. Through-hole mounting gives a very rugged construction and uses well established soldering methods. Surface mounting has the advantages of high packing density plus high-speed automated assembly.

AXIAL AND RADIAL LEADED DEVICES

The following general rules are for the safe handling and soldering of axial and radial leaded diodes. Special rules for particular types may apply and, for these, instructions are given in the individual data sheets. With all components, excessive forces or heat can cause serious damage and should always be avoided.

Handling

- Avoid perpendicular forces on the body of the diode
- Avoid sudden forces on the leads or body. These forces are often much greater than allowed
- Avoid high acceleration as a result of any shock, e.g. dropping the device on a hard surface
- During bending, support the leads between body or stud and the bending point
- During the bending process, axial forces on the body must not exceed 20 N
- Bending the leads through 90° is allowed at any distance from the body when it is possible to support the leads during bending without contacting the body or weldings
- Bending close to the body or stud without supporting the leads is only allowed if the bend radius is greater than 0.5 mm
- Twisting the leads is allowed at any distance from the body or stud only if the lead is properly clamped between body or stud and the twisting point
- Without clamping, twisting the leads is allowed only at a distance of greater than 3 mm from the body; the torque angle must not exceed 30°
- Straightening bent leads is allowed only if the applied pulling force in the axial direction does not exceed 20 N and the total pull duration is not longer than 5 s.

Soldering

- Avoid any force on the body or leads during or immediately after soldering
- Do not correct the position of an already soldered device by pushing, pulling or twisting the body
- Avoid fast cooling after soldering.

The maximum allowable soldering time is determined by:

- Package type
- Mounting environment
- Soldering method
- Soldering temperature
- Distance between the point of soldering and the seal of the component body.

The maximum permissible temperature of the solder is 260 °C; this temperature must not be in contact with the joint for more than 5 s. The total contact time of successive solder waves must not exceed 5 s.

The component may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified storage maximum. If the PCB has been preheated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

Mounting

If the rules for handling and soldering are observed, the following mounting or process methods are allowed:

- Preheating of the printed-wiring board before soldering up to a maximum of 100 °C
- Flat mounting with the diode body in direct contact with the printed-wiring board with or without metal tracks on both sides and/or plated-through holes
- Flat mounting with the diode body in direct contact with hot spots or hot tracks during soldering
- Upright mounting with the diode body in direct contact with the printed-wiring board if the body is not in contact with metal tracks or plated-through holes.

Repairing soldered joints

Apply the soldering iron to the component pin(s) below the seating plane, or not more than 2 mm above it. If the temperature of the soldering iron bit is below 300 °C, it may remain in contact for up to 10 s. If it is over 300 °C but below 400 °C, it may only remain in contact for up to 5 s.

Soldering guidelines and SMD footprint design

Chapter 4

SURFACE-MOUNT DEVICES

Since the introduction of surface mount devices (SMDs), component design and manufacturing techniques have changed almost beyond recognition. Smaller pitch, minimum footprint area and reduced component volume all contribute to a more compact circuit assembly. As a consequence, when designing PCBs, the dimensions of the footprints are perhaps more crucial than ever before.

One of the first steps in this design process is to consider which soldering method, either wave or reflow, will be used during production. This determines not only the solder footprint dimensions, but also the minimum spacing between components, the available area underneath the component where tracks may be laid, and possibly the required component orientation during soldering.

Although reflow soldering is recommended for SMDs, many manufacturers use, and will continue to use for some time to come, a mixture of surface-mount and through-hole components on one substrate (a mixed print).

The mix of components affects the soldering methods that can be applied. A substrate having SMDs mounted on one or both sides but no through-hole components is likely to be suitable for reflow or wave soldering. A double sided mixed print that has through-hole components and some SMDs on one side and densely packed SMDs on the other normally undergoes a sequential combination of reflow and wave soldering. When the mixed print has only through-hole components on one side and all SMDs on the other, wave soldering is usually applied.

To help with your circuit board design, this guideline gives an overview of both reflow and wave soldering methods, and is followed by some useful hints on hand soldering for repair purposes, and the recommended footprints for our SMD discrete semiconductor packages.

Reflow soldering process

There are three basic process steps for single-sided PCB reflow soldering, these are:

1. Applying solder paste to the PCB
2. Component placement
3. Reflow soldering.

APPLYING SOLDER PASTE TO THE PCB

Solder paste can be applied to the PCBs solder lands by one of either three methods: dispensing, screen or stencil printing.

Dispensing is flexible but is slow, and only suitable for pitches of 0.65 mm and above.

With screen printing, a fine-mesh screen is placed over the PCB and the solder paste is forced through the mesh onto the solder lands of the PCB. However, because of mesh aperture limitations (emulsion resolution), this method is only suitable for solder paste deposits of 300 μm and wider.

Stencil printing is similar to screen printing, except that a metal stencil is used instead of a fine-mesh screen. The stencil is usually made of stainless steel or bronze and should be 150 to 200 μm thick. A squeegee is passed across the stencil to force solder paste through the apertures in the stencil and onto the solder lands on the PCB (see Fig.1). It does not suffer from the same limitations as the other two printing methods and so is the preferred method currently available.

It is recommended that for solder paste printing, the equipment is located in a controlled environment maintained at a temperature of 23 ±2 °C, and a relative humidity between 45% and 75%.

Soldering guidelines and SMD footprint design

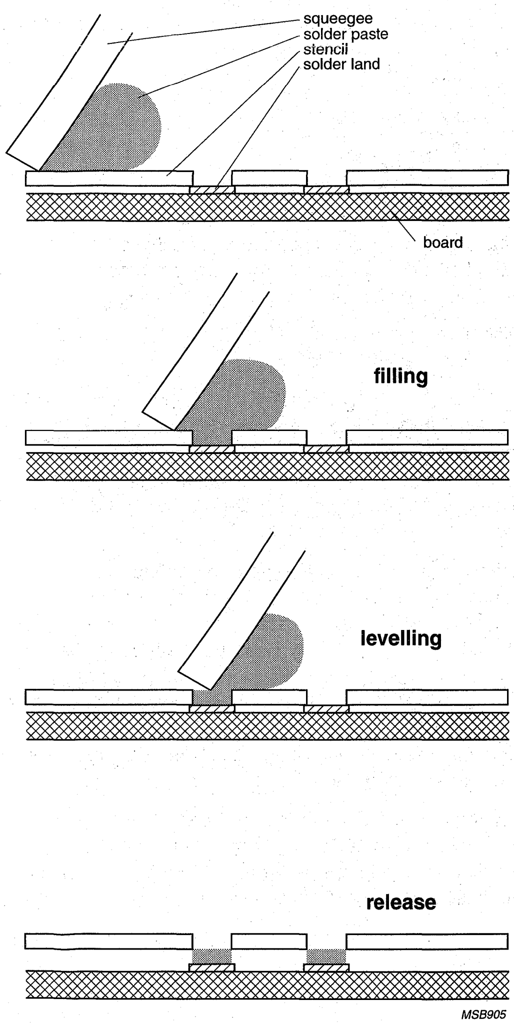


Fig.1 Applying solder paste by stencilling.

Stencil printing

The printing process must be able to apply the solder paste deposits to the PCB:

- In the correct amounts
- At the correct position on the lands
- With an acceptable height and shape.

The amount of solder paste used must be sufficient to give reliable soldered joints. This amount is controlled by the stencil thickness, aperture dimensions, process settings, and the volume of paste pressed through the apertures by the squeegee.

The downward force of the squeegee is counteracted by the hydrodynamic pressure of the paste, and so the machine should be set to ensure that the stencil is just 'cleaned' by the squeegee.

Suitable aperture dimensions depend on the stencil thickness. The solder paste deposits must have a flat part on the top (Fig.2, examples 4 and 5), which can be achieved by correct process settings. The footprints given in this book were designed for these correct deposit types. Stencil apertures that are too small result in irregular dots on the lands (Fig.2, examples 1 to 3). If the apertures are too large, solder paste can be scooped out, particularly if a rubber squeegee is used (Fig.2, example 6).

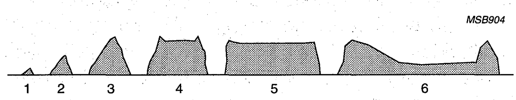


Fig.2 Shapes of solder deposits for increasing stencil apertures (left to right).

Ideally, the deposited solder paste should sit entirely on the solder land. The tolerated misplacement of solder paste with respect to the solder land is determined by the most critical component. The solder paste deposit must be deposited within 100 μm with respect to the solder land.

Furthermore, the tackiness (tack strength) of the solder paste must be sufficient to hold surface-mount devices on the PCB during assembly and during transport to the reflow oven. Tack strength depends on factors such as paste composition, drying conditions, placement pressure, dwell time and contact area. As a general rule, component placement should be within four hours after the paste printing process.

Squeegee

The squeegee can be either metal or rubber. A metal squeegee gives better overall results and so is recommended, however with step stencils, a rubber squeegee has to be used. The footprints given in this chapter were designed for application by both types of squeegee.

Soldering guidelines and SMD footprint design

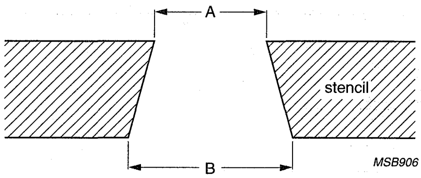
Stencil apertures

Stencil apertures can be made by either:

- Etching
- Laser cutting
- Electroforming.

Of the three methods, etching is less accurate as the deviation in aperture dimensions with respect to the target is relatively large (target is +50 μm at squeegee side and 0 μm at PCB side).

Laser-cut and electroformed stencils have smaller deviations in dimensions and are therefore more suitable for small and fine-pitch components (see Fig.3).



A = B +0/−30 (μm).
B = X ±30 (μm).
X = nominal apertures size.

Fig.3 Specifications of laser-cut stencil apertures for discrete and passive components.

A useful method of controlling the stencil printing process during production is by monitoring the weight of solder paste on the board which may vary between 80% and 110% of the theoretical amount according to the target (designed) apertures. Smearing and clogging of a small aperture cannot be detected with this method.

Solder paste

Reflow soldering uses a paste consisting of small nodules of solder and a flux with binder, solvents and additives to control rheological properties. The flux in the solder paste can be rosin mildly activated or rosin activated.

The requirements of the solder paste are:

- Good rolling behaviour
- No slump during heat-up
- Low viscosity during printing
- High viscosity after printing
- Sufficient tackiness to hold the components
- Removal of oxides during reflow soldering.

Suitable solder paste types have the following compositions:

- Sn62Pb36Ag2
- Sn63Pb37
- Sn60Pb40.

COMPONENT PLACEMENT

The position of the component with respect to the solder lands is an important factor in the final result of the assembly process. A misaligned component can lead to unreliable joints, open circuits and/or bridges between leads.

The placement accuracy is defined as the maximum permissible deviation of the component outline or component leads, with respect to the actual position of the solder land pattern belonging to that component or component leads on the circuit board (see Fig.4).

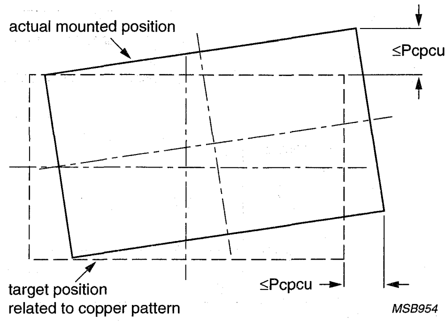


Fig.4 Component placement tolerances.

A maximum placement deviation (P) of 0.25 mm is used in these guidelines, which relates to the accuracy of a low-end placement machine. A higher placement accuracy is required for components with a fine pitch. This is given in the footprint description for the components concerned.

Besides the position in x- and y-directions, the z-position with respect to the solder paste, which is determined by the placement force, is also important. If the placement force is too high, solder paste will be squeezed out and solder balls or bridges will be formed. If the force is too low, physical contact will be insufficient, leads will not be soldered properly and the component may shift.

REFLOW SOLDERING

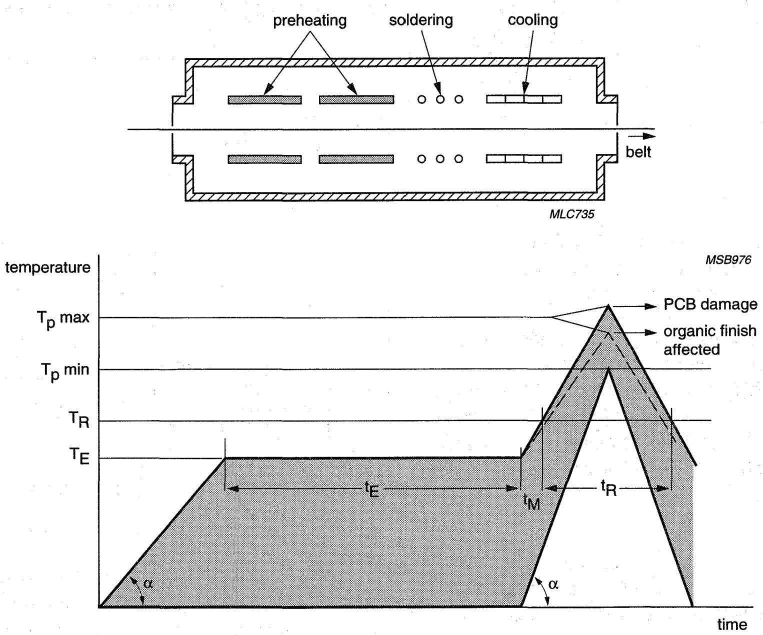
There are several methods available to provide the heat to reflow the solder paste, such as convection, hot belt, hot gas, vapour phase and resistance soldering. The preferred method is, however, convection reflow.

Convection reflow

With this method, the PCBs passes through an oven where it is preheated, reflow soldered and cooled (see Fig.5). If the heating rate of the board and components are similar, however, preheating is not necessary.

During the reflow soldering process, all parts of the board must be subjected to an accurate temperature/ time profile. Figure 5 shows a suitable profile framework for single-sided reflow soldering and the first side of double-sided print boards. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

Reflow soldering can be done in either air or a nitrogen atmosphere. If soldering in air, the temperature (T_p) must not exceed 240 °C on the first side of a double-sided print board with organic coated solder lands. This is because peak temperatures greater than 240 °C reduce the solderability of the lands on the second side to be soldered. This peak temperature can rise to 280 °C when soldering the second side with organic coated solder lands in air.



α	≤ 10 °C/s.	t_E	≤ 1 min, if possible (else ≤ 5 min).
T_E	≤ 160 °C.	t_M	= 2 to 30 s.
T_R	= 180 °C.	t_R	≤ 70 s.
$T_P$min	= 205 °C.		
$T_p$max	= 240 °C		for soldering the first side of a double-sided board with organic finish.
$T_P$max	= 280 °C		for all other cases.

Fig.5 Convection reflow soldering method (top), process requirements for reflow soldering (bottom).

Soldering guidelines and SMD footprint design

Chapter 4

If soldering in a nitrogen atmosphere, a peak temperature of 280 °C is allowed for double-sided print boards or single-sided reflow soldering. Soldering in a nitrogen atmosphere results in smoother joint meniscus, smaller contact angles, and better wetting of the copper solder lands.

The profile can be achieved by correct combinations of conveyor speed and heater temperature. To check whether the profile is within specification, the coldest and hottest spots on the board have to be located.

To do this, you should dispense solder paste deposits regularly over the surface of a test board and on the component leads. Set the oven to a moderate temperature with maximum conveyor velocity and pass the test board through. If too many solder paste dots melt, lower the oven's temperature. Continue passing test boards through the oven, while lowering the speed of the belt in small steps.

The deposit that melts first indicates the warmest location, the one that melts last indicates the coldest location. Paste dots not reflowed after two runs must be replaced by fresh dots. Thermocouples have to be mounted at the coldest and warmest location and temperature profiles measured.

Double-wave soldering process

There are four basic process steps for double-wave soldering, these are:

1. Applying adhesive
2. Component placement
3. Curing adhesive
4. Wave soldering process.

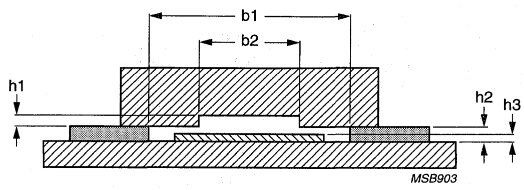
Applying adhesive

To hold SMDs on the board during wave soldering, it is necessary to bond the component to the PCB with one or more adhesive dots. This is done either by dispensing, stencilling or pin transfer. Dispensing is currently the most popular technique. It is flexible and allows a controlled amount of adhesive to be applied at each position. Stencil printing and pin transfer are less flexible and are mainly used for mass production. The component-specific requirements for an adhesive dot are:

- Shape (volume) of the adhesive dot
- Number of dots per component
- Position of the dots.

Volume of adhesive

There must be enough adhesive to keep components in their correct positions while being transported to the curing oven. This means that the deposited adhesive must be higher than the gap between the component and the board surface. Nevertheless, there should not be too much deposit as it may smear onto the solder lands, where it can affect their solderability. The gap between a component and printed board depends on the geometry of the board and component (see Fig.6).



h1 = component stand-off height.
h2 = solder resist (and track) height on PCB.
h3 = copper height on PCB.
b1 = gap between solder lands on the PCB.
b2 = gap between metallization of the component.

Fig.6 Available space for adhesive between component and PCB (unmarked area).

Table 1 gives guidelines for volumes of adhesive dots per package. The spreading in volumes should be within ±15%.

Table 1 Guidelines for volumes of adhesive dots

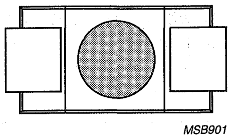
COMPONENT	NUMBER OF DOTS	VOLUME PER DOT (mm^3)
SOD106	1	0.65
SOD80C, SOD87	1 2	0.5 0.08
SOD110, SOD323	2	0.065
SOT323 (SC70-3)	2	0.045
SOT23, SOT143, SOT 346 (SC59)	2	0.06
SOT89	2	0.3
SOT223	2	0.70

Soldering guidelines and SMD footprint design

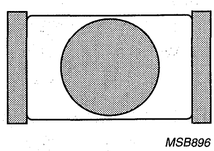
Chapter 4

Number, position and volume of dots per component

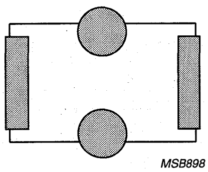
Figure 7 shows the recommended positions and numbers of adhesive dots for a variety of packages. SOD106, SOT89 and SOT223 packages require much larger adhesive dots compared with those for other components. SOD80C and SOD87 packages can have one large adhesive dot (recommended) or two smaller adhesive dots.



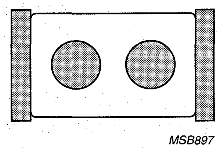
a. SOD106.



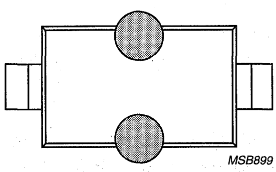
b. SOD80C, SOD87.



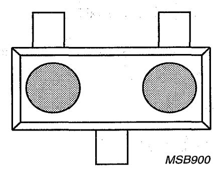
c. SOD110.



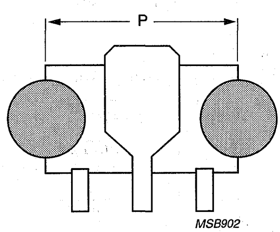
d. SOD80C, SOD87.



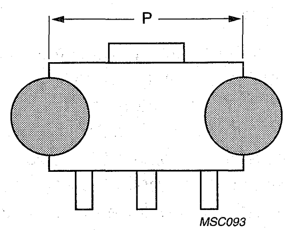
e. SOD323.



f. SOT23, SOT143, SOT323 (SC70-3) SOT346 (SC59).



g. SOT89 (P = 4.4 mm).



h. SOT223 (P = 6.0 mm).

For optimum power dissipation, the SOT89 requires a good thermal contact (i.e. good solder joint) between the package and the solder land. During wave-soldering, however, flux may not always reach the total soldering area beneath the component body, which in turn can lead to an incomplete solder joint. If the SOT89 is double-wave soldered, therefore, power derating must be applied.

Fig.7 Position of adhesive dots. Pitch between two small dots is 1.0 mm.

Soldering guidelines and SMD footprint design

Nozzle outlet diameter

Depending on adhesive type and component size, the nozzle outlet diameter of the dispenser can vary between 0.6 and 0.7 mm for the larger dots, and between 0.3 and 0.5 mm for the smaller dots.

As the rheology of the adhesive is temperature dependent, the temperature in the nozzle must be carefully controlled before dispensing. The required temperature depends on the adhesive type, but is usually between 26 °C and 32 °C to maintain the adhesive's rheology within specification during dispensing. Thermally curing epoxy adhesives are normally used.

Adhesives

Beside the nozzle diameters, different adhesive types are also used for different component sizes. Small components can be secured during assembly and wave soldering with a thin (low green strength) adhesive, which can be dispensed at high speeds. For larger components (such as QFP and SO packages), a higher green strength adhesive is required.

COMPONENT PLACEMENT

Positioning components on the PCB is similar in practice to that of reflow soldering.

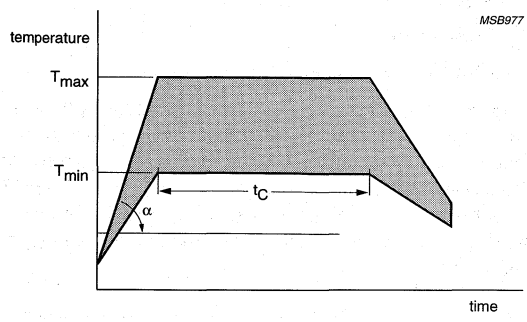
To prevent component shift and smearing of the adhesive, board support is important while placing components. This is particularly important when placing the SOD106 package.

CURING THE ADHESIVE

To provide sufficient bonding strength between component and board, the adhesive must be properly cured. Figure 8 gives general process requirements for curing most thermosetting epoxy adhesives with latent hardeners. The temperature profile of all adhesive dots on the PCB must be within this framework. It's important to note that this profile is for discrete semiconductor packages. The actual framework for the entire PCB could be smaller than the one shown, as other components on the board may have different process requirements.

To check whether the profile is within specification, the temperature of coldest and hottest spots must be measured. The coldest spot is usually under the largest package: the hottest spot is usually under the smallest package.

The adhesive can be cured either by infrared or hot-air convection.



T_{max} ≤ 160 °C.
T_{min} ≥ 110 °C.
t_C ≥ 3 minutes.
α ≤ 100 °C/min (some adhesives allow higher heating rates).
If T_{min} > 125 °C, t_C may be <3 min, depending on adhesive specification.

Fig.8 Process requirements for curing thermosetting adhesives.

Bonding strength

The bonding strength of glued components on the board can be checked by measuring the torque force. For small components the requirements are given in Table 2.
No values are specified for larger packages.

Table 2 Bonding strength requirements

COMPONENT	MINIMUM BONDING STRENGTH (cNcm)	TARGET BONDING STRENGTH (cNcm)
SOD323, SOD110, SOT323 (SC70-3)	110	250
SOD80C, SOD87	200	350
SOT23, SOT346 (SC59), SOT143	150	250

Soldering guidelines and SMD footprint design

Chapter 4

WAVE SOLDERING PROCESS

After applying adhesive, placing the component on the PCB and curing, the PCB can be wave soldered. The wave soldering process is basically built up from three sub-processes. These are:

1. Fluxing
2. Preheating
3. (Double) wave soldering.

Although listed here as sub-process they are in practice combined in one machine. All are served by one transport mechanism, which guides the PCBs at an incline through the soldering machine. It's important to note that the PCB must be loaded into the machine so that the SMDs on the board come into direct contact with the solder wave (see Fig.9).

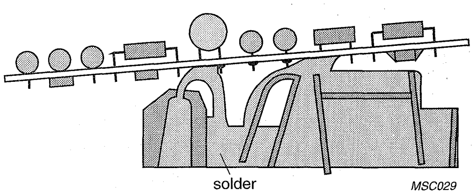


Fig.9 Double-wave soldering.

In principle, two different systems of PCB transports are available for wave soldering:

- Carrier transport

  PCBs are mounted on a soldering carrier, which moves through the soldering machine, taking it from one sub-process to the next. The advantage of carrier mounting is that the board is fixed and warpage during soldering is reduced.

- Carrierless transport

  PCBs are guided through the soldering machine by a chain with grips. This method is more convenient for mass production.

Fluxing

Fluxing is necessary to promote wetting both of the PCB and the mounted components. This ensures a good and even solder joint.

During the fluxing process, the solder side of the PCB (including the components) are covered with a thin layer of solder flux, which can be applied to the PCB either by spraying or as a foam. Although several types of solder flux are available for this purpose, they can be categorized into three main groups:

- Non-activated flux (e.g. rosin-based fluxes)
- Mildly activated flux (e.g. rosin-based or synthetic fluxes)
- Highly activated flux (e.g. water-soluble fluxes).

The choice for a particular flux type depends mainly on the products to be soldered.

Although there is always some flux residue left on the PCB after soldering, it's not always necessary to wash the boards to remove it. Whether to clean the board can depend on:

- The type of flux used (highly activated fluxes are corrosive and so should always be removed).
- The required appearance of the board after soldering.
- Customer requirements.

Preheating

After the flux is applied, the PCB needs to be preheated. This serves several purposes: it evaporates the flux solvents, it accelerates the activity of the flux and it heats the PCB and components to reduce thermal shock.

The required pre-heat temperature depends on the type of flux used. For example, the more common low-residue fluxes require a pre-heat temperature of 120 °C (measured on the wave solder side of the PCB).

(Double) wave soldering

The PCB first passes over a highly intensive (jet) solder wave with a carefully controlled constant height. This ensures good contact with the PCB, the edges of SMDs and the leads of components near to high non-wetted bodies. The greater the board's immersion depth into this first wave, the fewer joints will be missed.

If the PCB is carrier mounted, the first wave's height, and thus the board's immersion depth, can be greater. Carrierless soldering is more convenient for mass production, but the height of the wave must be lower to avoid solder overflowing to the top side of the board. The height of the jet wave is given in Table 3 along with an indication of soldering process window. This information is based on a 1.6 mm thick PCB.

Table 3 Process ranges for carrierless and carrier double wave soldering

	CARRIERLESS	CARRIER
Preheat temperature of board at wave solder side (°C)	120 ±10	
Heating rate preheating (°C/s)	$\Delta T/\Delta t \leq 3$	
First (jet) wave: wave height with respect to bottom side of board (mm)	1.6 +0.5/–0	3.0 +0.5/–0
Second (laminar) wave (double sided overflow): height with respect to underside of the board (mm) relative stream velocity with respect to the board	0.8 +0.5/–0 0	
Solder temperature (°C)	250 ±3	
Contact times (s): first (jet) wave second (laminar) wave	0.5 +0.5/–0 2.0 ±0.2 (plain holes); 2.5 ±0.2 (plated holes)	
PCB transport angle (°)	7 ±0.5	
Solder alloys	Sn60Pb40; Sn60Pb38Bi2	

The second, smoother laminar solder wave completes formation of the solder fillet, giving an optimal soldered connection between component and PCB. It also reduces the possibility of solder bridging by taking up excessive solder.

To reduce lead/tin oxides and possibly other solder imperfection forming during soldering, the complete wave configuration can be encapsulated by an inert atmosphere such as nitrogen.

Hand soldering microminiature components

It is possible to solder microminiature components with a light-weight hand-held soldering iron, but this method has obvious drawbacks and should be restricted to laboratory use and/or incidental repairs on production circuits:

- Hand-soldering is time-consuming and therefore expensive
- The component cannot be positioned accurately and the connecting tags may come into contact with the substrate and damage it
- There is a risk of breaking the substrate and internal connections in the component could be damaged
- The component package could be damaged by the iron.

Assessment of soldered joint quality

The quality of a soldered joint is assessed by inspecting the shape and appearance of the joint. This inspection is normally done with either a low-powered magnifier or microscope, however where ultra-high reliability is required, video, X-ray or laser inspection equipment may be considered.

Both sides of the PCB should be carefully examined: there should be no misaligned, missing or damaged components, soldered joints should be clean and have a similar appearance, there should be no solder bridging or residue, and the PCB should be assessed for general cleanliness.

Unlike leaded component joints where the lead also provides added mechanical strength, the SMD relies on the quality of the soldering for both electrical and mechanical integrity. It is therefore necessary that the inspector is trained to make a visual assessment with regard to long-term reliability.

Criteria used to assess the quality of an SMD solder joint include:

- Correct position of the component on the solder lands
- Good wetting of the surfaces
- Correct amount of solder
- A sound, smooth joint surface.

Soldering guidelines and SMD footprint design

Chapter 4

POSITIONING

If a lead projects over the solder land too far an unreliable joint is obtained. Figures 10 to 12 show the maximum shift allowed for various components. The dimensions of these solder lands guarantee that, in the statistically extreme situation, a reliable soldered joint can be made.

GOOD WETTING

This produces an even flow of solder over the surface land and component lead, and thinning towards the edges of the joint. The metallic interaction that takes place during soldering should give a smooth, unbroken, adherent layer of solder on the joint.

CORRECT AMOUNT OF SOLDER

A good soldered joint should have neither too much nor too little solder: there should be enough solder to ensure electrical and mechanical integrity, but not so much that it causes solder bridging.

SOUND, SMOOTH JOINT SURFACE

The surface of the solder should be smooth and continuous. Small irregularities on the solder surface are acceptable, but cracks are unacceptable.

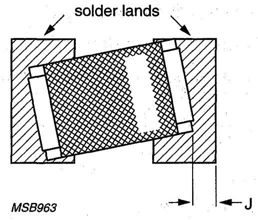


Fig.10 J ≥ 0.3 mm.

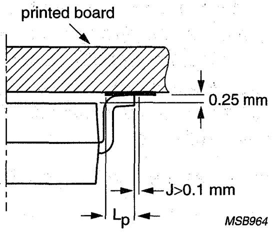


Fig.11 J ≥ 0.1 mm; solder land > L_p.

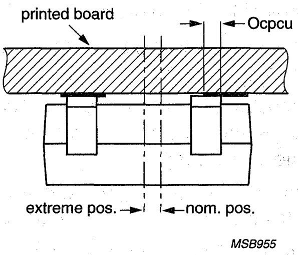


Fig.12 Oc > half lead width.

Soldering guidelines and SMD footprint design

Chapter 4

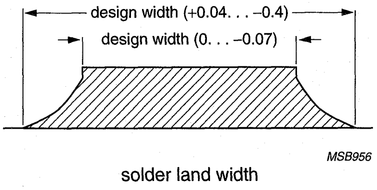
Footprint definitions

A typical SMD footprint, is composed of:

- Solder lands (conductive pattern)
- Solder resist pattern
- Occupied area of the component
- Solder paste pattern (for reflow soldering only)
- Area underneath the SMD available for tracks
- Component orientation during wave soldering.

SOLDER LANDS (CONDUCTIVE PATTERN)

The dimensions of the solder lands given in these guidelines are the actual dimensions of the conductive pattern on the printed board (see Fig.13).
These dimensions are more crucial for fine-pitch components.



The solder land dimensions are designed to give optimum soldering results. They do not take into account the copper area for optimum power dissipation. If an extra area is required to improve power dissipation, it should be coated with solder resist. This is especially important for power packages such as SOD106, SOT89 and SOT223.

Fig.13 Requirements of solder land dimensions.

SOLDER RESIST PATTERN

The solder resist on the circuit board prevents short circuits during soldering, increases the insulation resistance between adjacent circuit details and stops solder flowing away from solder lands during reflow soldering.

In contrast to the tracks, which must be entirely covered, solder lands must be free of solder resist. Because of this, the cut-outs in the solder resist pattern should be at least 0.15 mm or 0.3 mm larger than the relevant solder lands (for a photo-defined and screen printed solder resist pattern respectively). The solder resist cut-outs given with the footprints in these guidelines are sketched and their dimensions can be calculated by using the above rule. Consult your printed board supplier for agreement with these solder resist cut-outs.

OCCUPIED AREA OF THE COMPONENT

A minimum spacing between components is necessary to avoid component placement problems, short circuits during wave or reflow soldering and dry solder joints during wave soldering caused by non-wettable component bodies. These problems can be avoided by placing the components so the occupied areas do not overlap (see Fig.14).

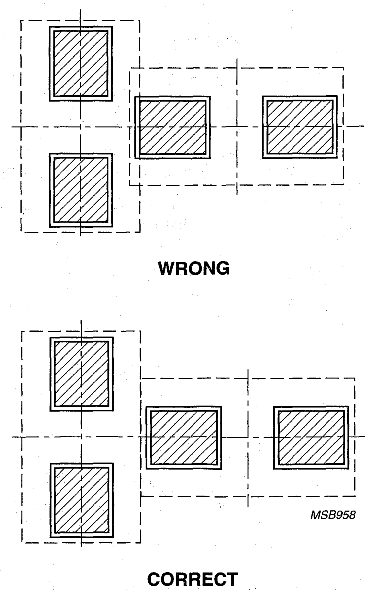


Fig.14 Minimum spacing required (bottom) between components.

Soldering guidelines and SMD footprint design

Chapter 4

SOLDER PASTE PATTERN

It is important to use a solder paste printer which is optical aligned with the PCBs copper pattern for the reflow footprints presented here. This is because, for these footprints, the solder paste deposit must be within a 0.1 mm tolerance with respect to the copper pattern.

To ensure the right amount of solder for each solder joint, the stencil apertures must be equal to the solder paste areas given by the footprints.

AREA AVAILABLE FOR TRACKS (CONDUCTIVE PATTERN)

Tracks underneath leadless SMDs must be covered with solder resist. However, as solder resist can sometimes be thin or have pin holes at the edges of tracks (especially when applied by screen printing), an additional clearance for tracks with respect to the actual metallization position of the mounted component should be taken into account (see Fig.15).

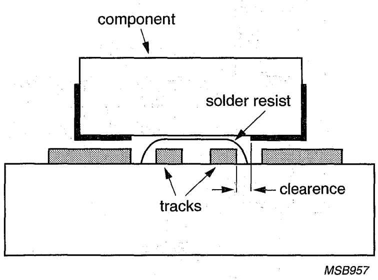


Fig.15 Clearance required underneath component between metallization and tracks.

For components that need the additional clearance, the footprints on the following pages give the maximum space for tracks not connected to the solder lands (clearance ≥ 0.1 mm), for low-voltage applications.
The number of tracks in this space is determined by the specified line resolution of the printed board.

COMPONENT ORIENTATION DURING WAVE SOLDERING

Where applicable, footprints for wave soldering are given with the transport direction of the PCB. This is given as either a 'preferred transport direction during soldering' or 'transport direction during soldering'.

Components with small terminals and non-wettable bodies, have a smaller risk of dry joints, especially when using carrierless soldering as the components are placed according to the 'preferred orientation'.

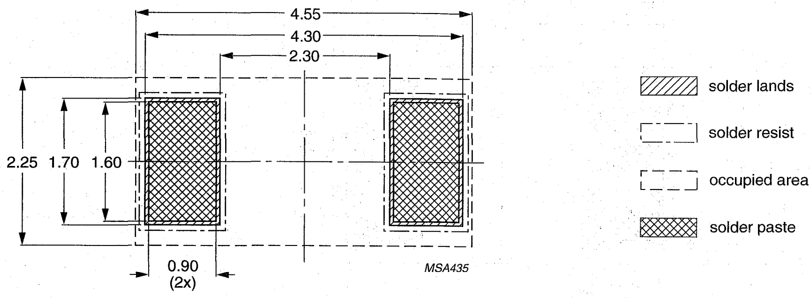
Components have no orientation preference for reflow soldering.

RECOMMENDED FOOTPRINTS

The recommended footprints for most of our discrete semiconductor packages are given on the following pages. For their dimensional outline drawings, refer to Chapter 2: Package outlines.

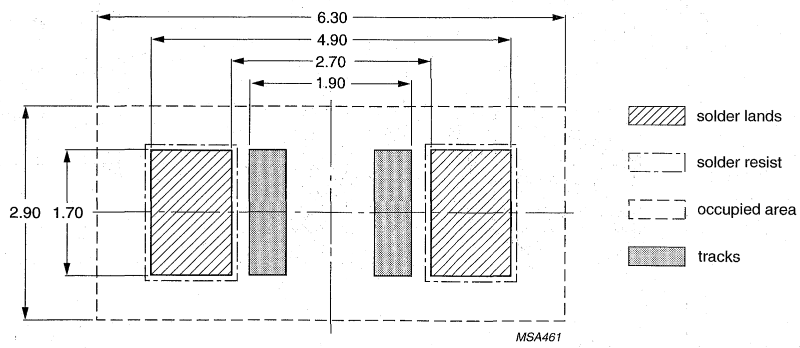
Soldering guidelines and SMD footprint design

Chapter 4



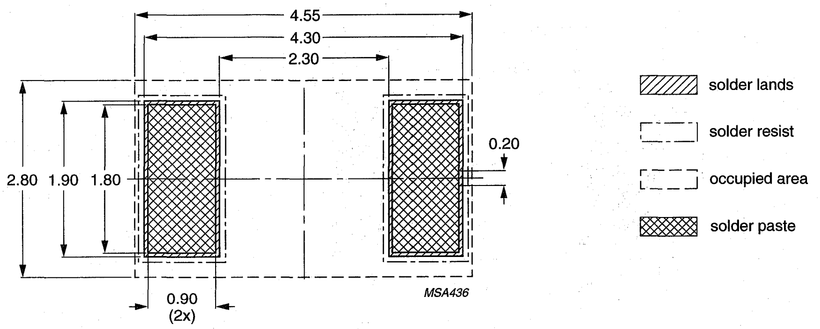
Dimensions in mm.

Fig.16 Reflow soldering footprint for SOD80C.



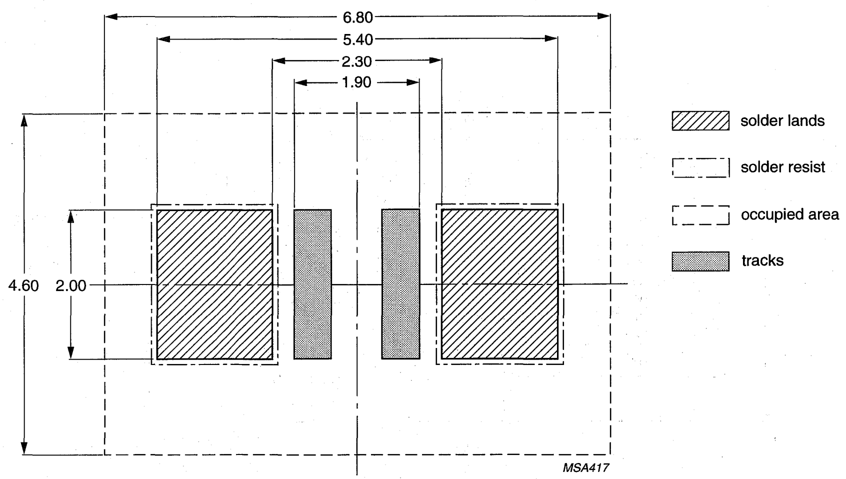
Dimensions in mm.

Fig.17 Wave soldering footprint for SOD80C.



Dimensions in mm.

Fig.18 Reflow soldering footprint for SOD87.

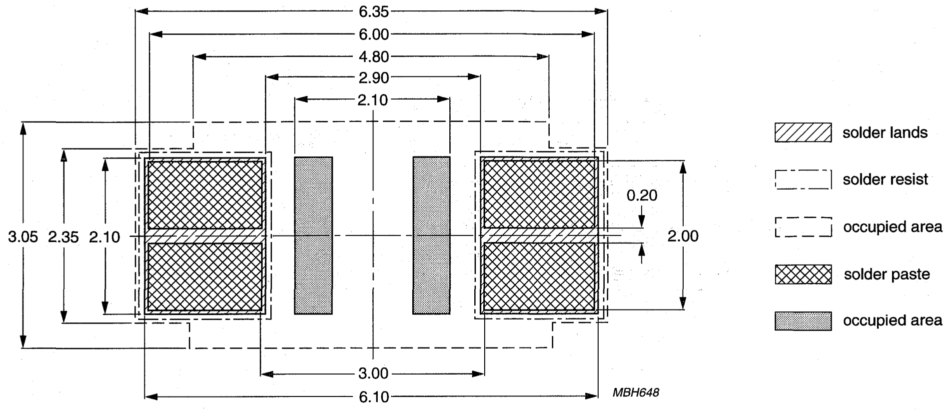


Dimensions in mm.

Fig.19 Wave soldering footprint for SOD87.

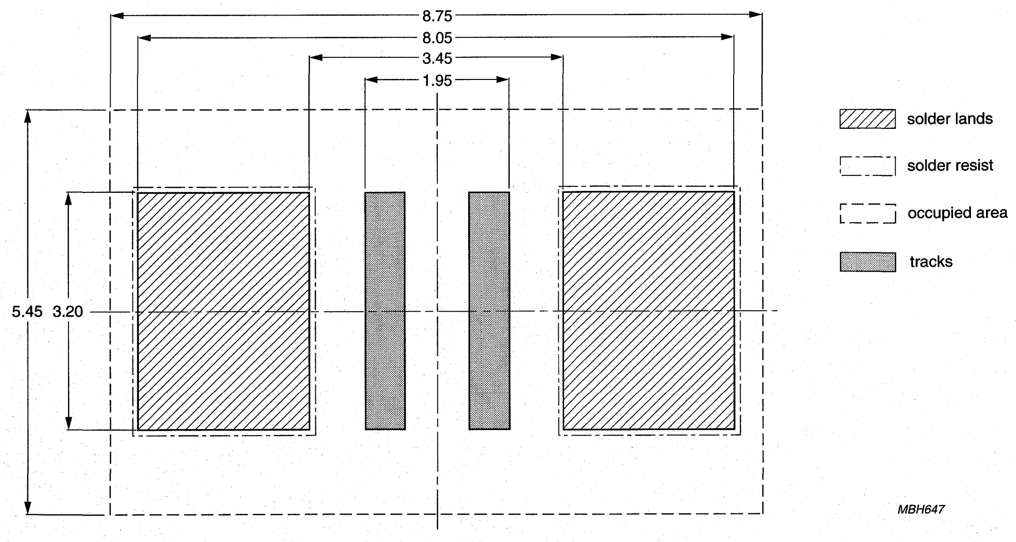
Soldering guidelines and SMD footprint design

Chapter 4



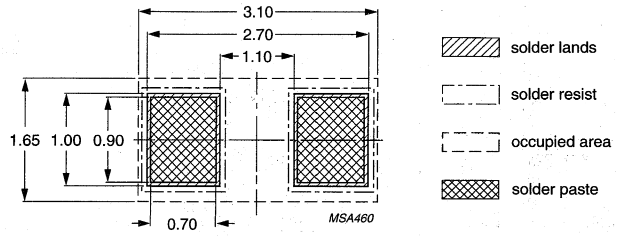
Dimensions in mm.

Fig.20 Reflow soldering footprint for SOD106.



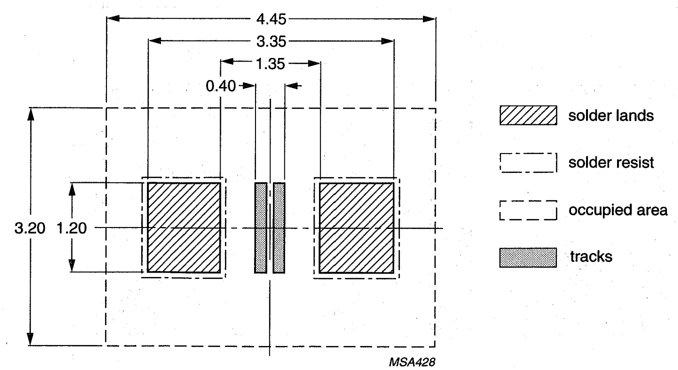
Dimensions in mm.

Fig.21 Wave soldering footprint for SOD106.



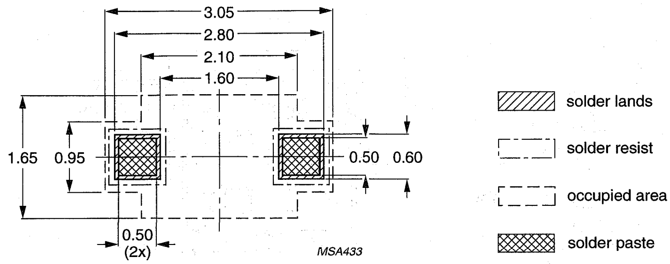
Dimensions in mm.

Fig.22 Reflow soldering footprint for SOD110.



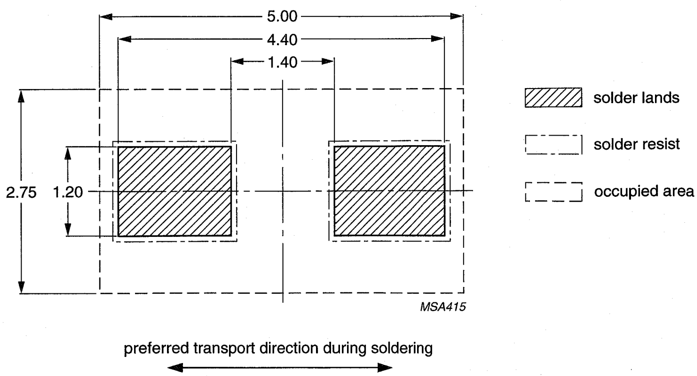
Dimensions in mm.

Fig.23 Wave soldering footprint for SOD110.



Dimensions in mm.

Fig.24 Reflow soldering footprint for SOD323 (SC-76).

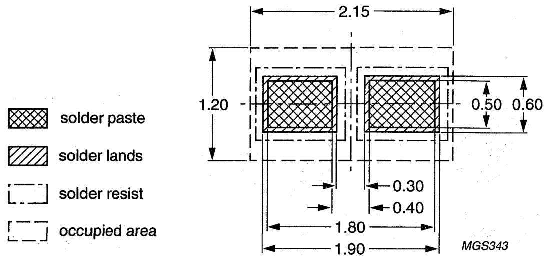


Dimensions in mm.

Fig.25 Wave soldering footprint for SOD323 (SC-76).

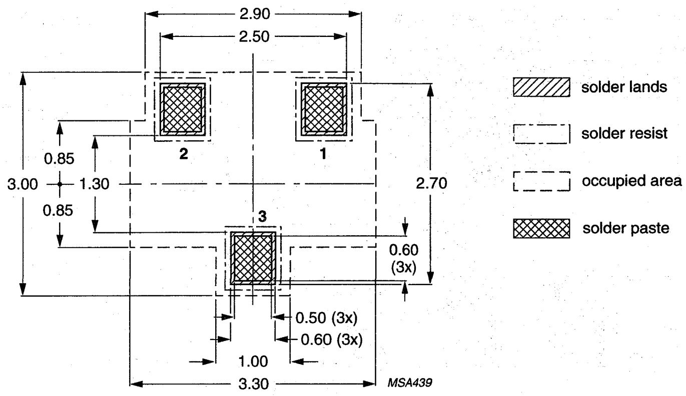
Soldering guidelines and SMD footprint design

Chapter 4



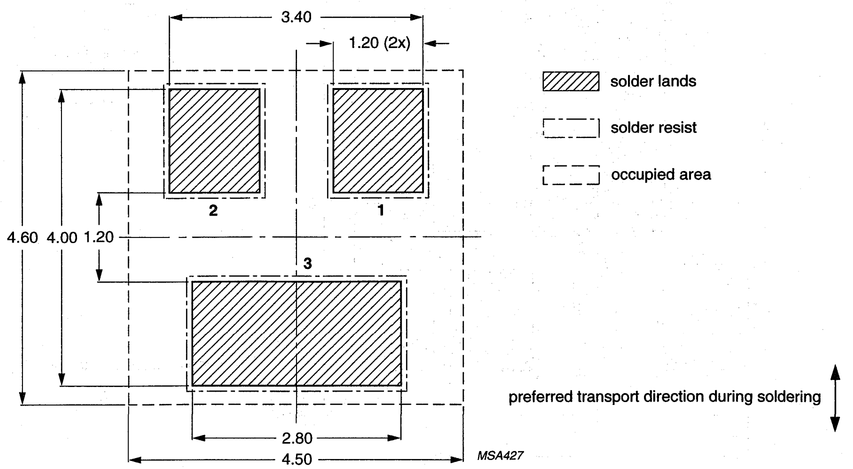
Dimensions in mm.

Fig.26 Reflow soldering footprint for SOD523 (not suitable for wave soldering).



Dimensions in mm.

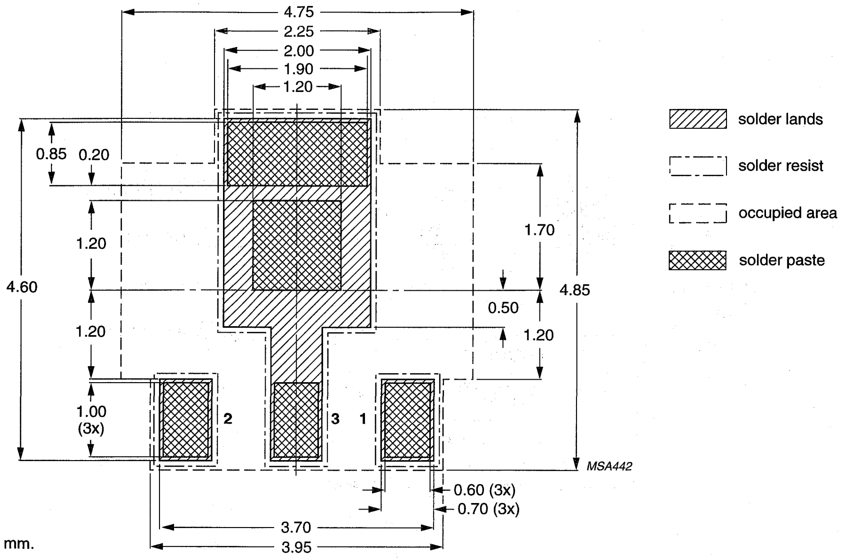
Fig.27 Reflow soldering footprint for SOT23.



Dimensions in mm.

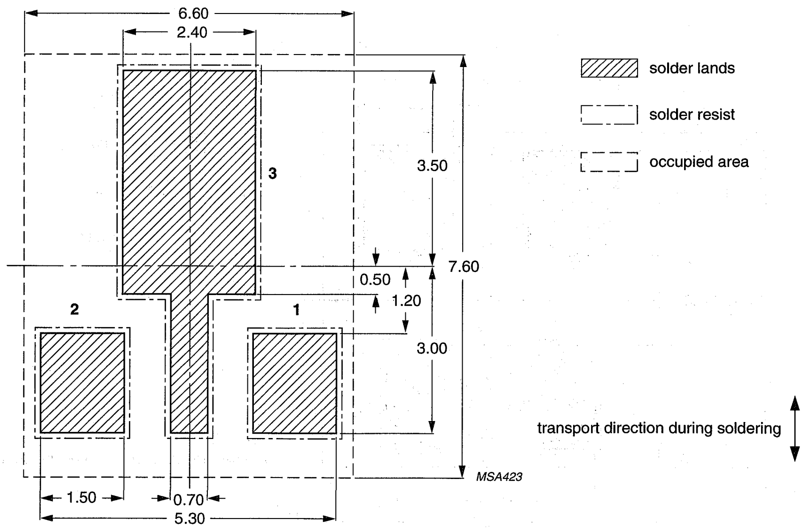
Fig.28 Wave soldering footprint for SOT23.

Soldering guidelines and SMD footprint design



Dimensions in mm.

Fig.29 Reflow soldering footprint for SOT89 (SC-62).



Dimensions in mm.

Not recommended for wave soldering (see Fig.7).

Fig.30 Wave soldering footprint for SOT89 (SC-62).

Dimensions (in mm)

	SOT96-1	SOT137-1
A =	6.60	11.0
B =	4.00	8.00
C =	1.30	1.50
F =	7.00	11.40
G =	5.50	16.00

placement accuracy
for all types = 0.25

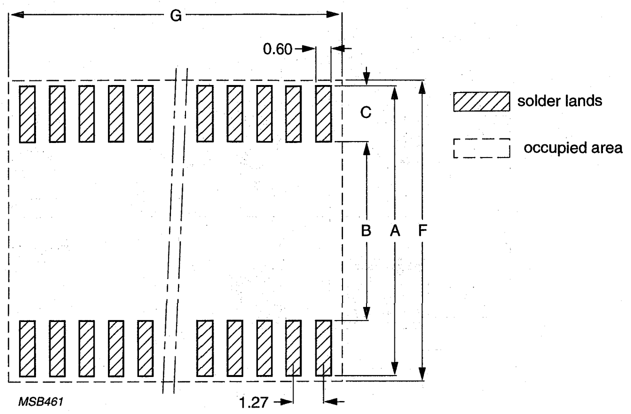


Fig.31 Reflow soldering footprint for SOT96-1 (SO8) and SOT137-1 (SO24).

Dimensions (in mm)

	SOT96-1	SOT137-1
N =	8 leads	24 leads
A =	8.00	11.50
B =	3.80	7.90
C =	2.10	1.80
F =	9.40	13.00
G =	7.10	18.50

placement accuracy
for all types = 0.25

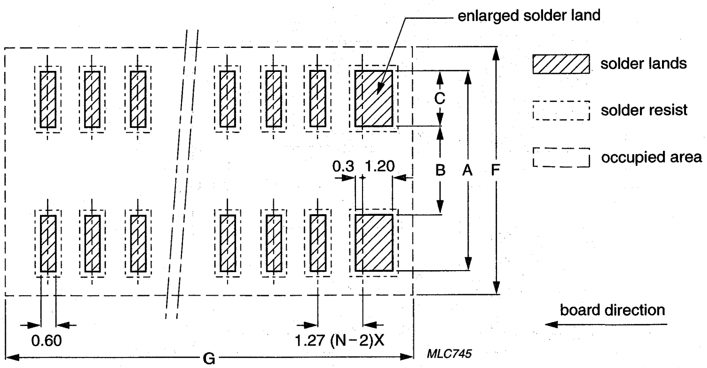
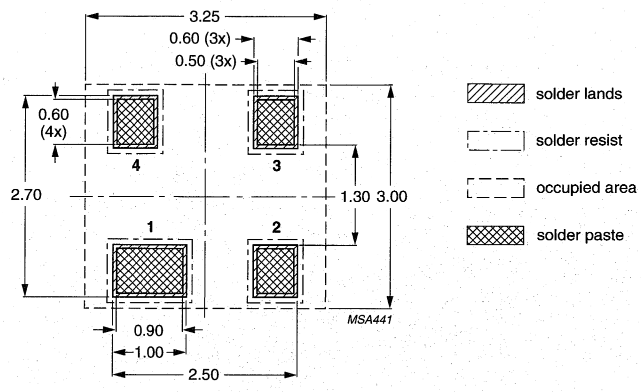
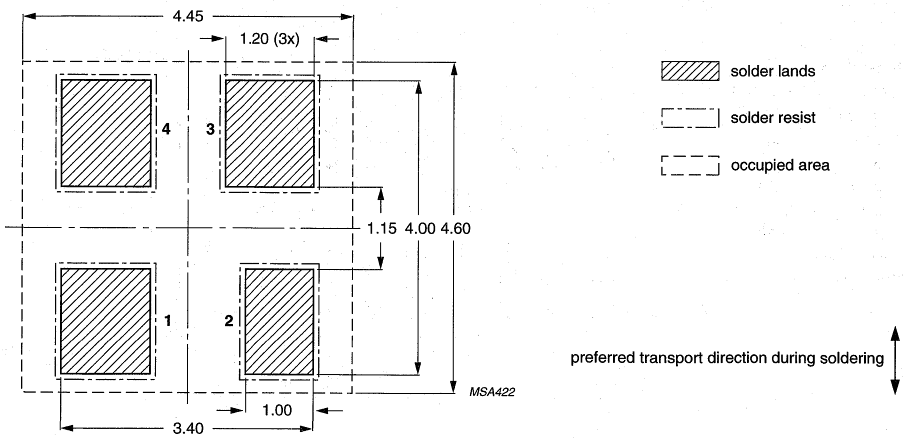


Fig.32 Wave soldering footprint for SOT96-1 (SO8) and SOT137-1 (SO24).



Dimensions in mm.

Fig.33 Reflow soldering footprint for SOT143B (footprint for SOT143R is mirror image).



Dimensions in mm.

Fig.34 Wave soldering footprint for SOT143B (footprint for SOT143R is mirror image).

Dimensions:
A = 11.00 mm
B = 8.00 mm
C = 1.50 mm
F = 11.40 mm
G = 13.40 mm
placement accuracy = 0.25 mm

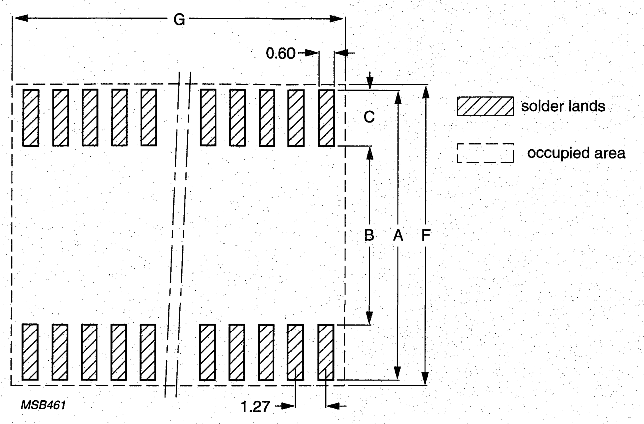


Fig.35 Reflow soldering footprint for SOT163-1 (SO20).

Dimensions:
A = 11.50 mm
B = 7.90 mm
C = 1.80 mm
F = 13.00 mm
G = 15.90 mm
N = 20 leads
placement accuracy = 0.25 mm

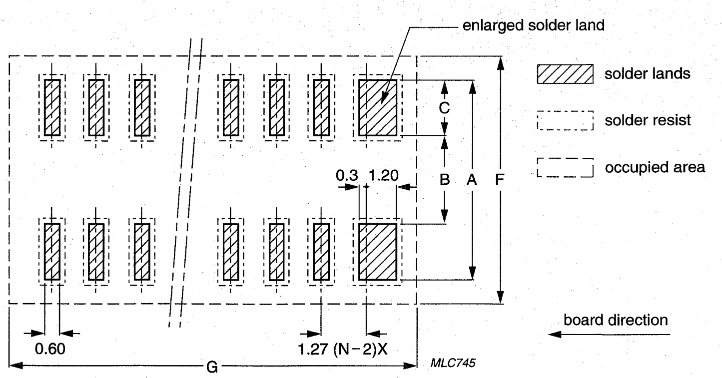
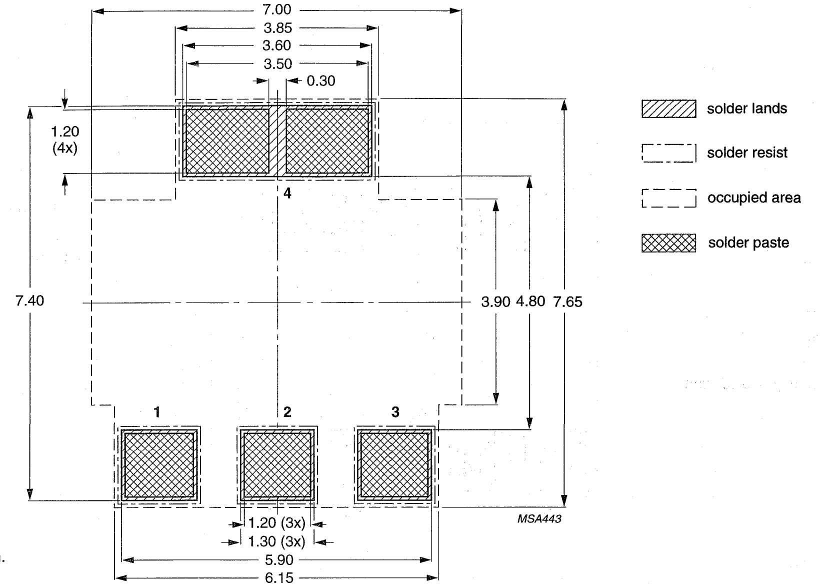
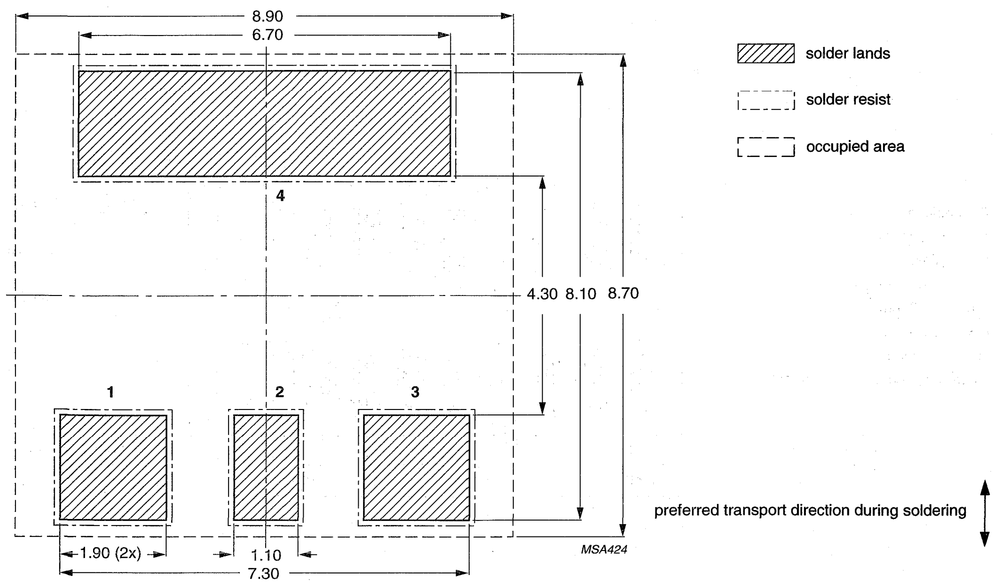


Fig.36 Wave soldering footprint for SOT163-1 (SO20).



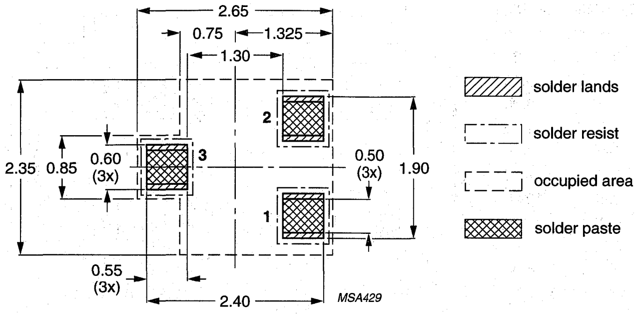
Dimensions in mm.

Fig.37 Reflow soldering footprint for SOT223 (SC-73).



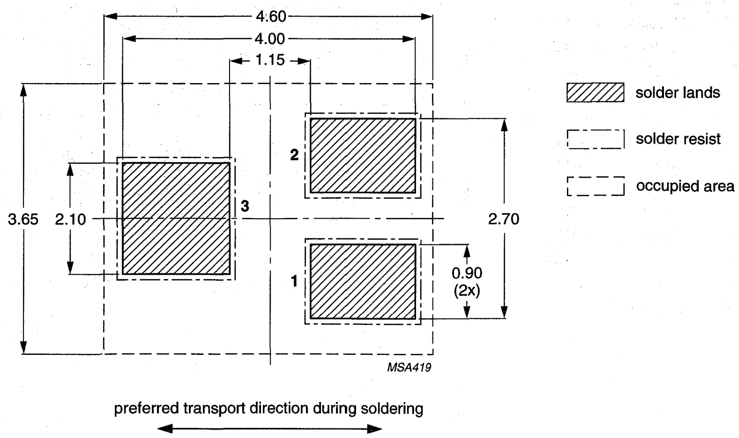
Dimensions in mm.

Fig.38 Wave soldering footprint for SOT223 (SC-73).



Dimensions in mm.

Fig.39 Reflow soldering footprint for SOT323 (SC-70).



Dimensions in mm.

Fig.40 Wave soldering footprint for SOT323 (SC-70).

Dimensions (in mm)

	SOT338-1	SOT339-1	SOT340-1	SOT341-1
N =	16 leads	20 leads	24 leads	28 leads
P =	0.65	0.65	0.65	0.65
A =	8.10	8.10	8.10	8.10
B =	5.70	5.90	5.90	5.90
C =	1.20	1.10	1.10	1.10
D =	0.40	0.40	0.40	0.40
F =	8.35	8.35	8.35	8.35
G =	6.50	7.50	8.50	10.50
H =	5.20	6.50	7.80	9.10
K =	5.55	5.55	5.55	5.60
M =	4.95	6.25	7.55	8.85

placement accuracy for all types = 0.15

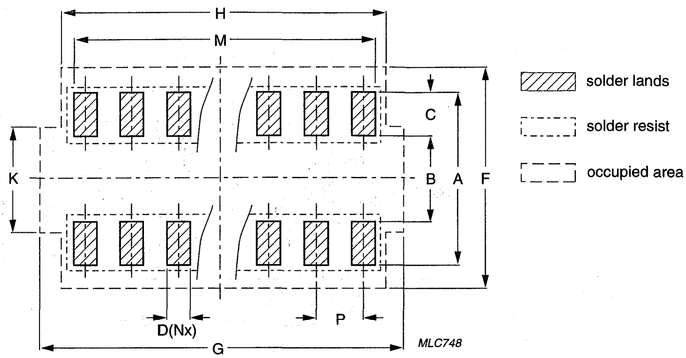


Fig.41 Reflow soldering footprint for SOT338-1 (SSOP16), SOT339-1 (SSOP20), SOT340-1 (SSOP24) and SOT34-1 (SSOP28).

Dimensions (in mm)

	SOT338-1	SOT339-1	SOT340-1	SOT341-1
N =	16 leads	20 leads	24 leads	28 leads
P =	0.65	0.65	0.65	0.65
A =	9.15	9.15	9.15	9.15
B =	5.35	5.55	5.55	5.55
C =	1.90	1.80	1.80	1.80
D =	0.30	0.30	0.30	0.30
F =	6.15	6.30	6.30	6.30
G =	10.65	10.80	10.80	10.80
H =	4.25	4.75	5.25	6.25
K =	7.075	7.725	8.375	9.025
M =	2.00	2.00	2.00	2.00

placement accuracy for all types = 0.10

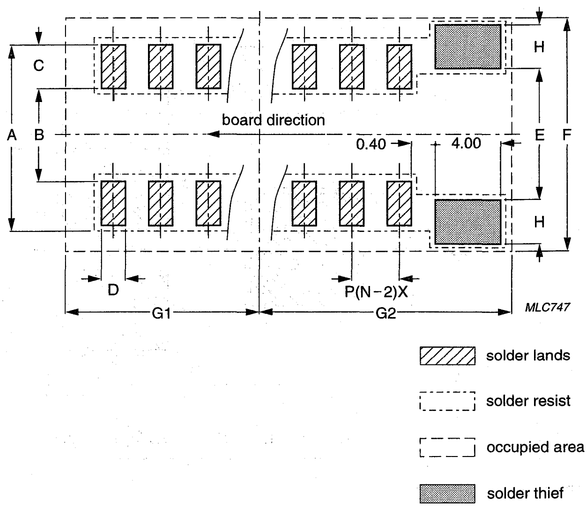
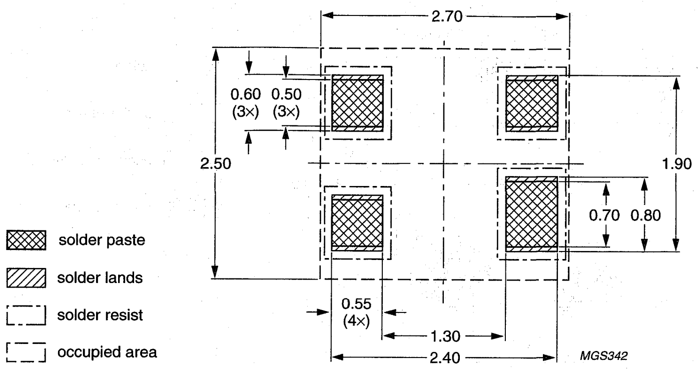
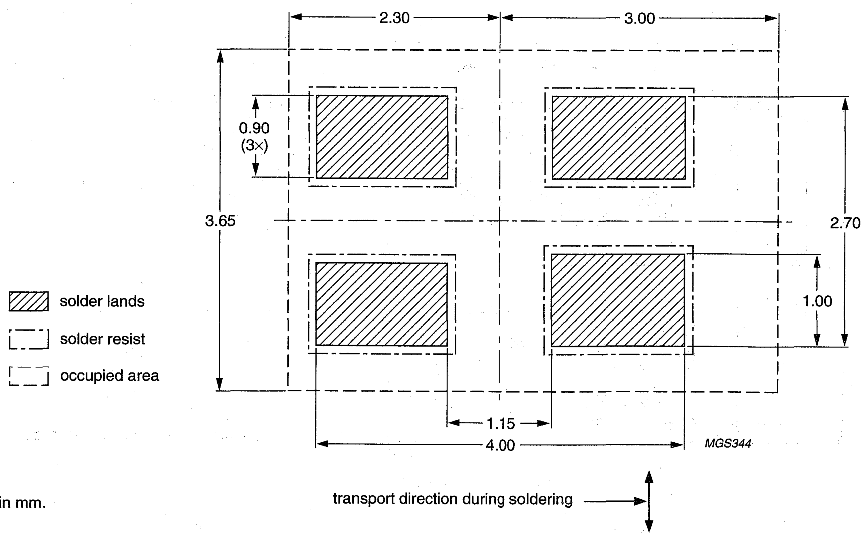


Fig.42 Wave soldering footprint for SOT338-1 (SSOP16), SOT339-1 (SSOP20), SOT340-1 (SSOP24) and SOT34-1 (SSOP28).



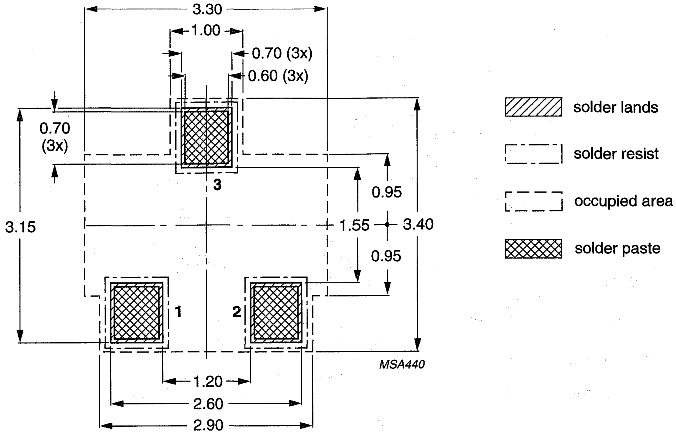
Dimensions in mm.

Fig.43 Reflow soldering footprint for SOT343N (footprint for SOT343R is mirror image).



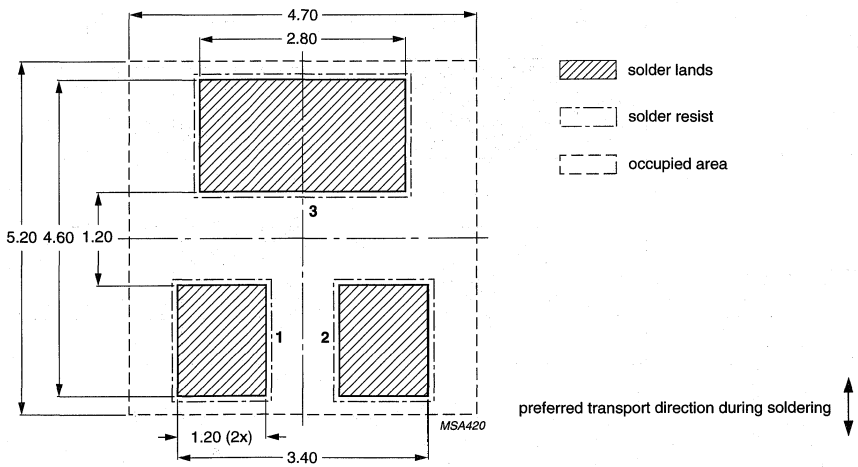
Dimensions in mm.

Fig.44 Wave soldering footprint for SOT343N (footprint for SOT343R is mirror image).



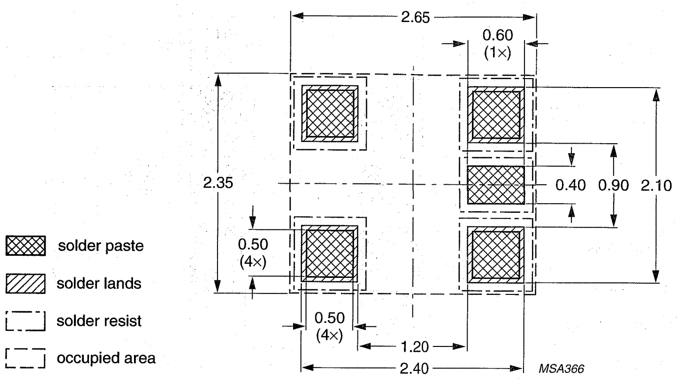
Dimensions in mm.

Fig.45 Reflow soldering footprint for SOT346 (SC-59).



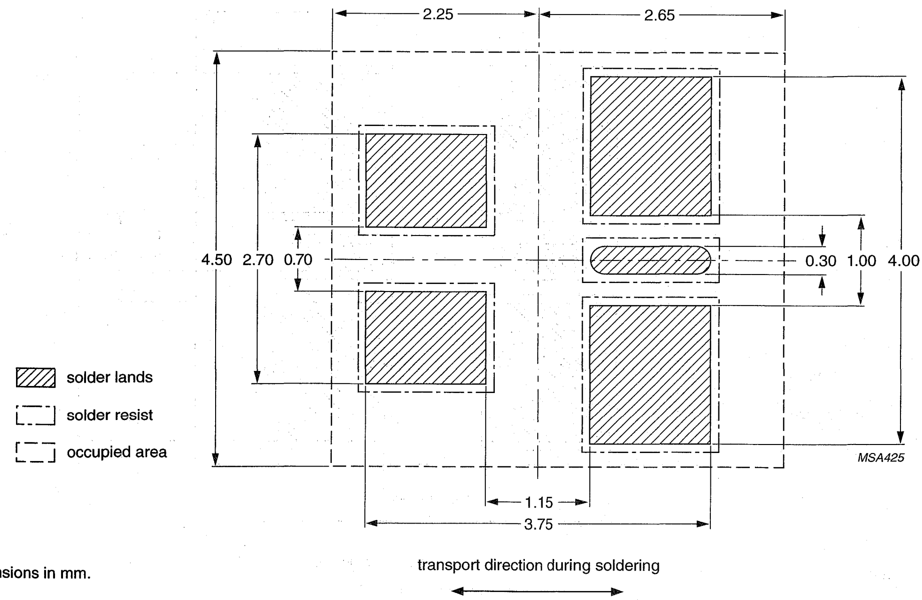
Dimensions in mm.

Fig.46 Wave soldering footprint for SOT346 (SC-59).



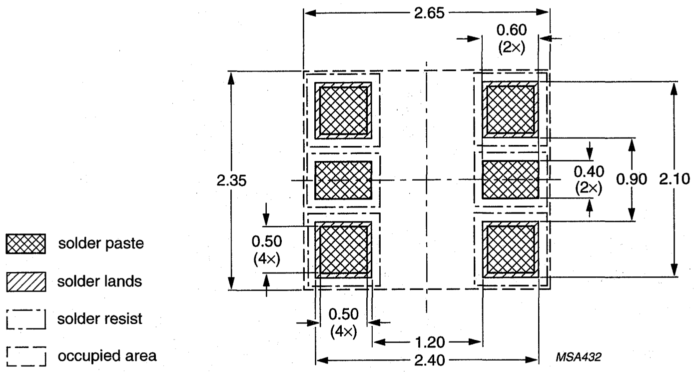
Dimensions in mm.

Fig.47 Reflow soldering footprint for SOT353 (SC-88A).



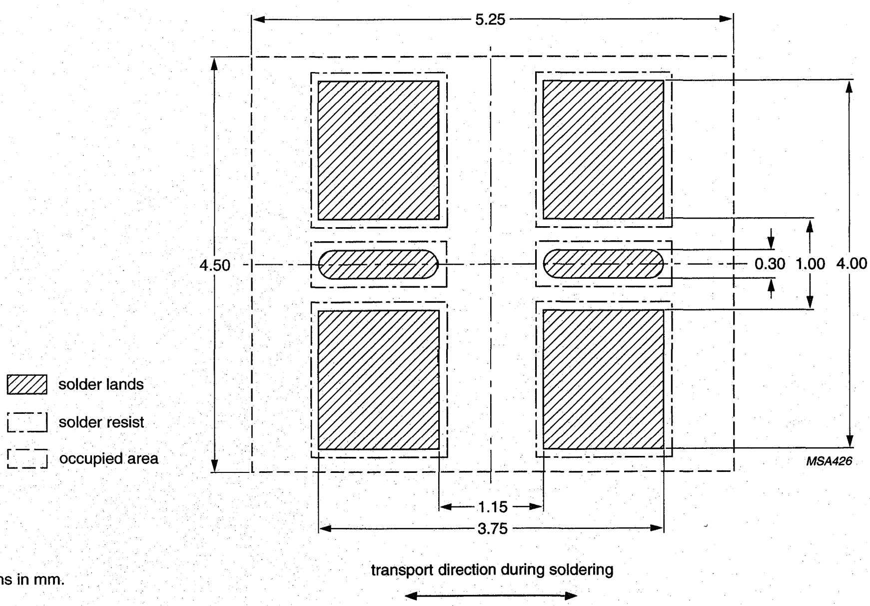
Dimensions in mm.

Fig.48 Wave soldering footprint for SOT353 (SC-88A).



Dimensions in mm.

Fig.49 Reflow soldering footprint for SOT363 (SC-88).

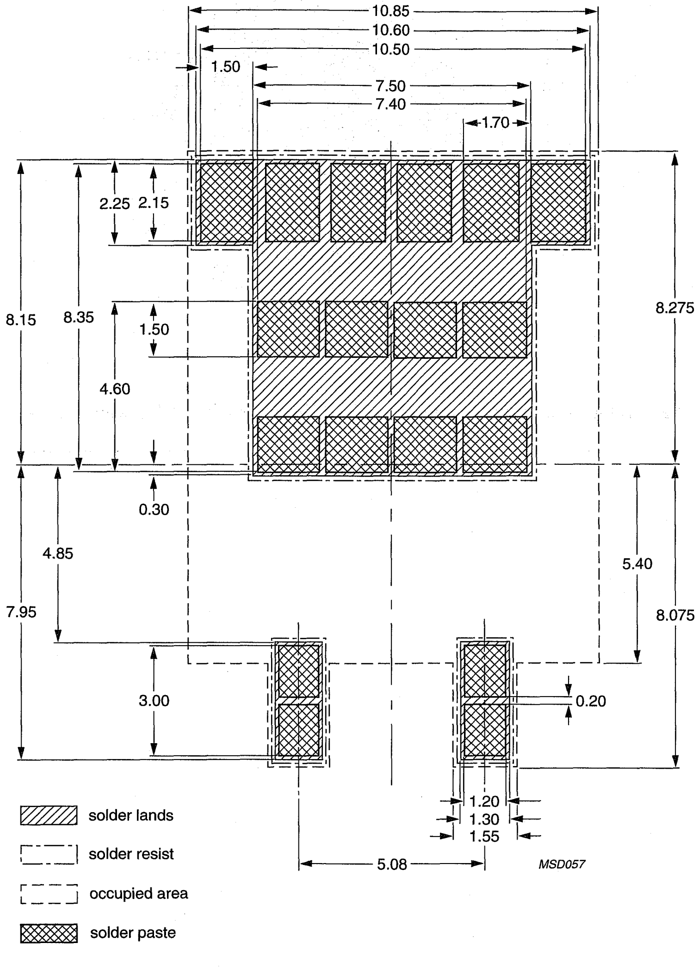


Dimensions in mm.

Fig.50 Wave soldering footprint for SOT363 (SC-88).

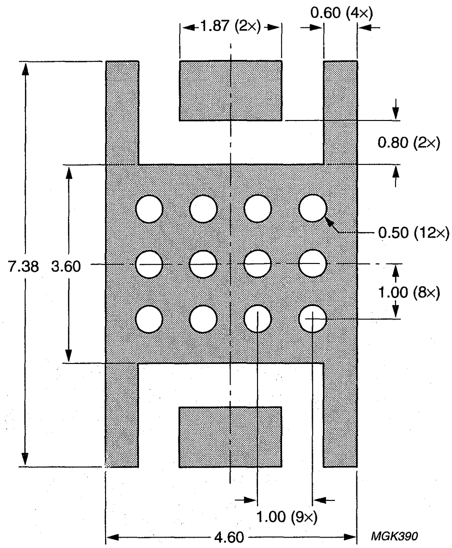
Soldering guidelines and SMD footprint design

Chapter 4



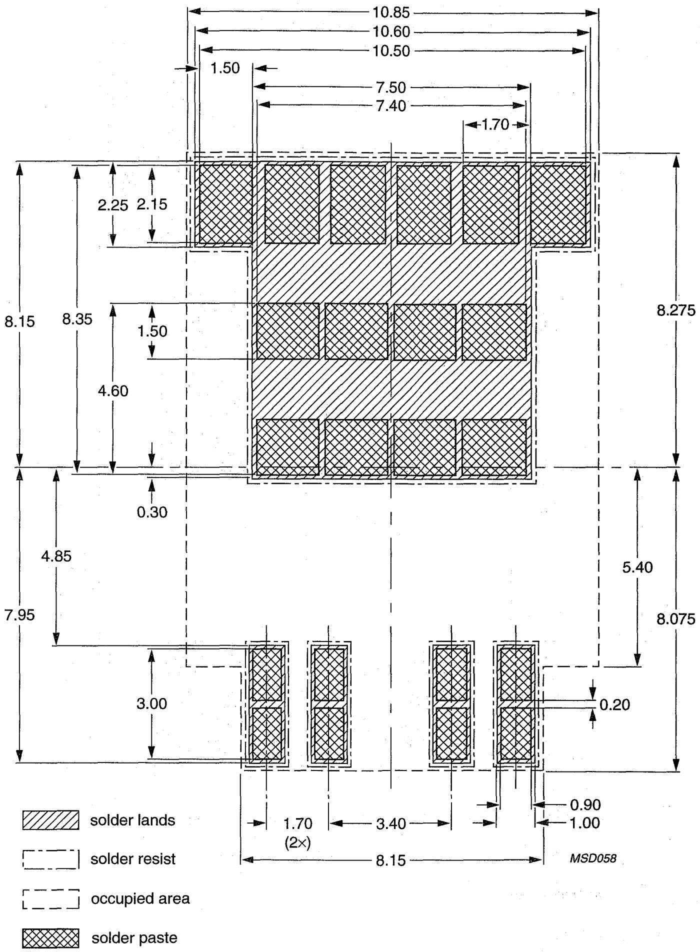
Dimensions in mm.

Fig.51 Reflow soldering footprint for SOT404.



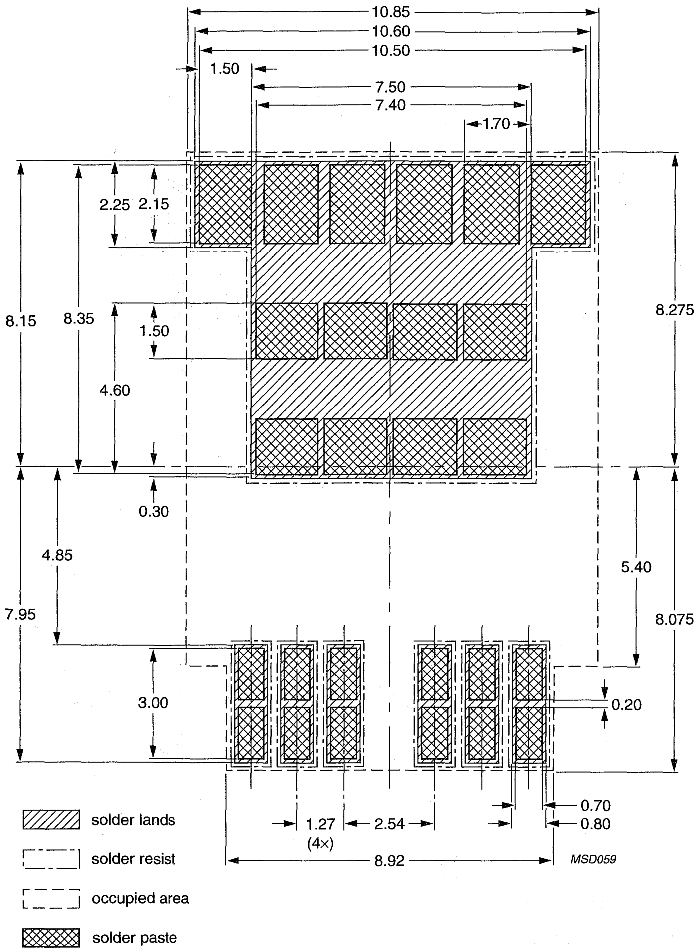
Dimensions in mm.

Fig.52 Reflow soldering footprint for SOT409A (not suitable for wave soldering).



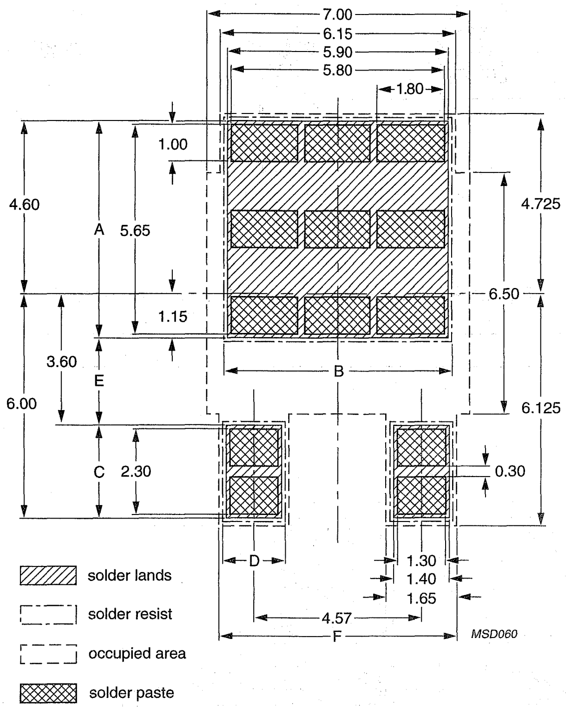
Dimensions in mm.

Fig.53 Reflow soldering footprint for SOT426.



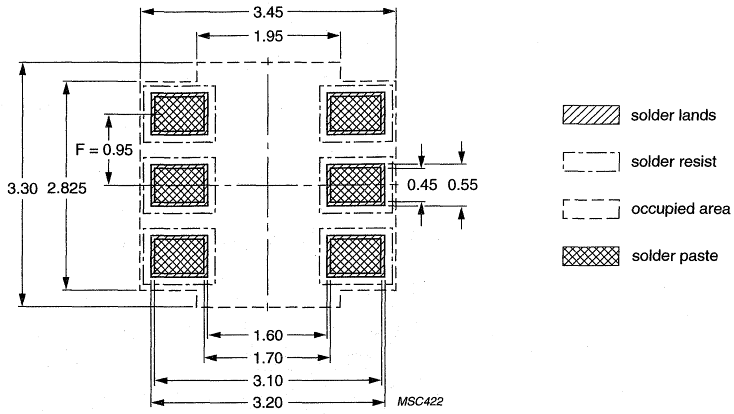
Dimensions in mm.

Fig.54 Reflow soldering footprint for SOT427.



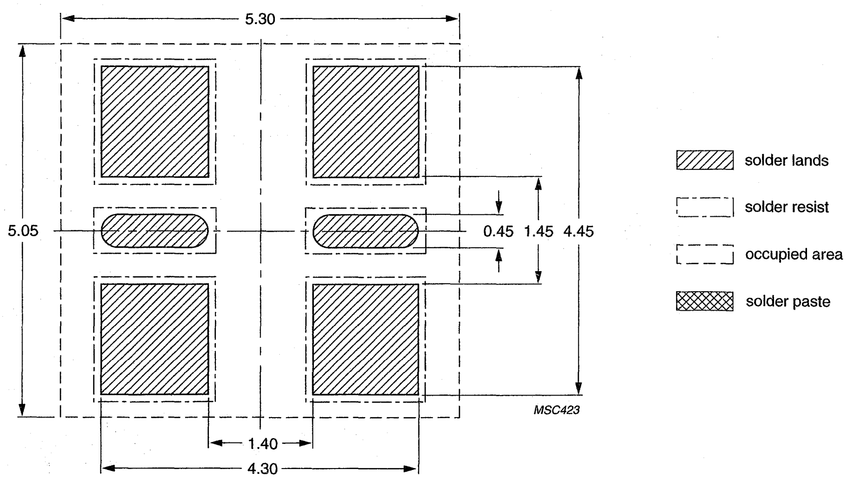
Dimensions in mm.

Fig.55 Reflow soldering footprint for SOT428.



Dimensions in mm.

Fig.56 Reflow soldering footprint for SOT457 (SC-74).



Dimensions in mm.

Fig.57 Wave soldering footprint for SOT457 (SC-74).

CHAPTER 5
THERMAL CONSIDERATIONS

Thermal considerations

Chapter 5

INTRODUCTION

The perfect power switch is not yet available. All power semiconductors dissipate power internally both during the on-state and during the transition between the on and off states. The amount of power dissipated internally generally speaking increases in line with the power being switched by the semiconductor. The capability of a switch to operate in a particular circuit will therefore depend upon the amount of power dissipated internally and the rise in the operating temperature of the silicon junction that this power dissipation causes. It is therefore important that circuit designers are familiar with the thermal characteristics of power semiconductors and are able to calculate power dissipation limits and junction operating temperatures.

This chapter is divided into three parts. Part One describes the essential thermal properties of semiconductors and explains the concept of a limit, in terms of continuous mode and pulse mode operation. Part Two gives worked examples showing junction temperature calculations for a variety of applied power pulse waveforms. Part Three discusses component heat dissipation and heatsink design.

PART ONE: THERMAL PROPERTIES

The power dissipation limit

The maximum allowable power dissipation forms a limit to the safe operating area of power transistors. Power dissipation causes a rise in junction temperature which will, in turn, start chemical and metallurgical changes. The rate at which these changes proceed is exponentially related to temperature, and thus prolonged operation of a power transistor above its junction temperature rating is liable to result in reduced life. Operation of a device at, or below, its power dissipation rating (together with careful consideration of thermal resistances associated with the device) ensures that the junction temperature rating is not exceeded.

All power semiconductors have a power dissipation limitation. For rectifier products such as diodes, thyristors and triacs, the power dissipation rating can be easily translated in terms of current ratings; in the on-state the voltage drop is well defined. Transistors are, however, somewhat more complicated. A transistor, be it a power MOSFET or a bipolar, can operate in its on-state at any voltage up to its maximum rating depending on the circuit conditions. It is therefore necessary to specify a Safe Operating Area (SOA) for transistors which specifies the power dissipation limit in terms of a series of boundaries in the current and voltage plane. These operating areas are usually presented for mounting base temperatures of 25 °C. At higher temperatures, operating conditions must be checked to ensure that junction temperatures are not exceeding the desired operating level.

Continuous power dissipation

The total power dissipation in a semiconductor may be calculated from the product of the on-state voltage and the forward conduction current. The heat dissipated in the junction of the device flows through the thermal resistance between the junction and the mounting base, $R_{thj\text{-}mb}$. The thermal equivalent circuit of Fig.1 illustrates this heat flow; P_{tot} can be regarded as a thermal current, and the temperature difference between the junction and mounting base $\Delta T_{j\text{-}mb}$ as a thermal voltage. By analogy with Ohm's law, it follows that:

$$P_{tot} = \frac{T_j - T_{mb}}{R_{thj-mb}} \quad (1)$$

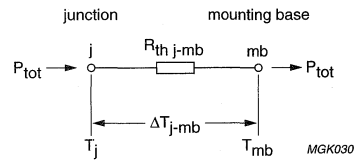


Fig.1 Heat transport in a transistor with power dissipation constant with respect to time.

Figure 2 shows the dependence of the maximum power dissipation on the temperature of the mounting base. P_{totmax} is limited either by a maximum temperature difference:

$$\Delta T_{j-mbmax} = T_{jmax} - T_{mbK} \quad (2)$$

or by the maximum junction temperature T_{jmax} ($T_{mb\,K}$ is usually 25 °C and is the value of T_{mb} above which the maximum power dissipation must be reduced to maintain the operating point within the safe operating area).

In the first case, $T_{mb} \le T_{mb\,K}$:

$$P_{totmaxK} = \frac{\Delta T_{j-mbmax}}{R_{thj-mb}} \quad (3)$$

that is, the power dissipation has a fixed limit value ($P_{tot\ max\ K}$ is the maximum DC power dissipation below $T_{mb\ K}$). If the transistor is subjected to a mounting-base temperature $T_{mb\ 1}$, its junction temperature will be less than T_{jmax} by an amount ($T_{mb\ K} - T_{mb\ 1}$), as shown by the broken line in Fig.2.

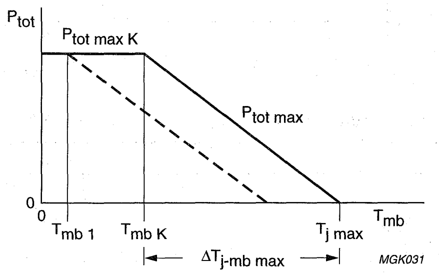


Fig.2 Maximum DC power dissipation in a transistor as a function of the mounting-base temperature.

In the second case, $T_{mb} > T_{mb\ K}$:

$$P_{totmax} = \frac{T_{jmax} - T_{mb}}{R_{thj-mb}} \qquad (4)$$

that is, the power dissipation must be reduced as the mounting base temperature increases along the sloping straight line in Fig.2. Equation (4) shows that the lower the thermal resistance $R_{thj\text{-}mb}$, the steeper is the slope of the line. In this case, T_{mb} is the maximum mounting-base temperature that can occur in operation.

Example

The following data is provided for a particular transistor.

$P_{tot\ max\ K} = 75$ W

$T_{jmax} = 175$ °C

$R_{thj\text{-}mb} \leq 2$ K/W

The maximum permissible power dissipation for continuous operation at a maximum mounting-base temperature of $T_{mb} = 80$ °C is required.

Note that the maximum value of T_{mb} is chosen to be significantly higher than the maximum ambient temperature to prevent an excessively large heatsink being required.

From Equation (4) we obtain:

$$P_{totmax} = \frac{175 - 80}{2}\ \text{W} = 47.5\ \text{W}$$

Provided that the transistor is operated within SOA limits, this value is permissible since it is below $P_{tot\ max\ K}$. The same result can be obtained graphically from the $P_{tot\ max}$ diagram (Fig.3) for the relevant transistor.

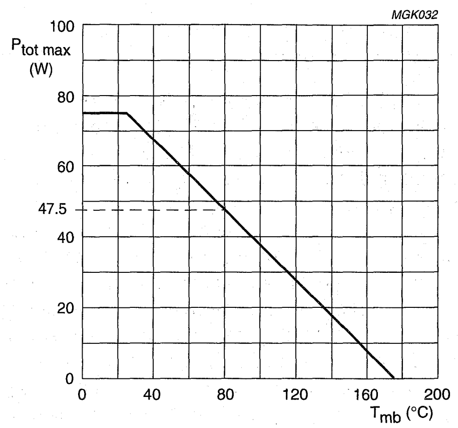


Fig.3 Example of the determination of maximum power dissipation.

Pulse power operation

When a power transistor is subjected to a pulsed load, higher peak power dissipation is permitted. The materials in a power transistor have a definite thermal capacity, and thus the critical junction temperature will not be reached instantaneously, even when excessive power is being dissipated in the device. The power dissipation limit may be extended for intermittent operation. The size of the extension will depend on the duration of the operation period (that is, pulse duration) and the frequency with which operation occurs (that is, duty factor).

Thermal considerations

Chapter 5

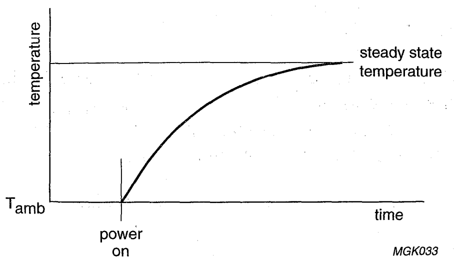


Fig.4 Heating of a transistor chip.

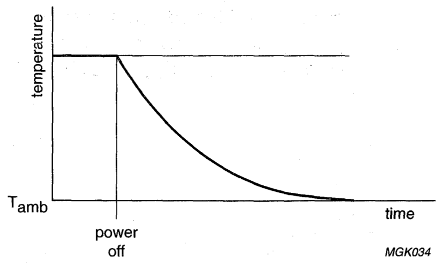


Fig.5 Heating and cooling follow the same law.

If power is applied to a transistor, the device will immediately start to warm up (see Fig.4). If the power dissipation continues, a balance will be struck between heat generation and removal resulting in the stabilization of T_j and $\Delta T_{j\text{-}mb}$. Some heat energy will be stored by the thermal capacity of the device, and the stable conditions will be determined by the thermal resistances associated with the transistor and its thermal environment. When the power dissipation ceases, the device will cool (the heating and cooling laws will be identical, see Fig.5). However, if the power dissipation ceases before the temperature of the transistor stabilizes, the peak values of T_j and $\Delta T_{j\text{-}mb}$ will be less than the values reached for the same level of continuous power dissipation (see Fig.6). If the second pulse is identical to the first, the peak temperature attained by the device at the end of the second pulse will be greater than that at the end of the first pulse. Further pulses will build up the temperature until some new stable situation is attained (see Fig.7). The temperature of the device in this stable condition will fluctuate above and below the mean. If the upward excursions extend into the region of excessive T_j then the life expectancy of the device may be reduced. This can happen with high-power low-duty-factor pulses, even though the average power is below the DC rating of the device.

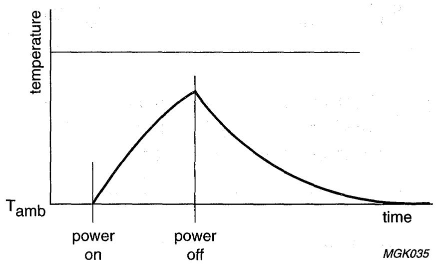


Fig.6 The peak temperature caused by a short power pulse can be less than steady-state temperature resulting from the same power.

Figure 8 shows a typical safe operating area for DC operation of a power MOSFET. The corresponding rectangular- pulse operating areas with a fixed duty factor, $\delta = 0$, and the pulse time t_p as a parameter, are also shown. These boundaries represent the largest possible extension of the operating area for particular pulse times. When the pulse time becomes very short, the power dissipation does not have a limiting action and the pulse current and maximum voltage form the only limits. This rectangle represents the largest possible pulse operating area.

Thermal considerations Chapter 5

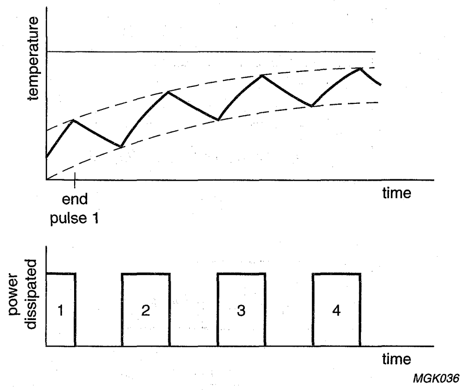


Fig.7 A train of power pulses increases the average temperature if the device does not have time to cool between pulses.

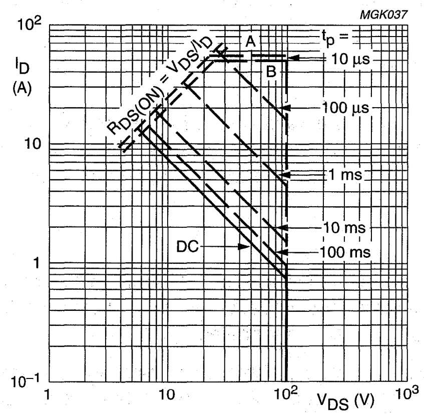


Fig.8 DC and rectangular pulse operating areas with fixed parameters $\delta = 0$, t_p and $T_{mb} = 25$ °C.

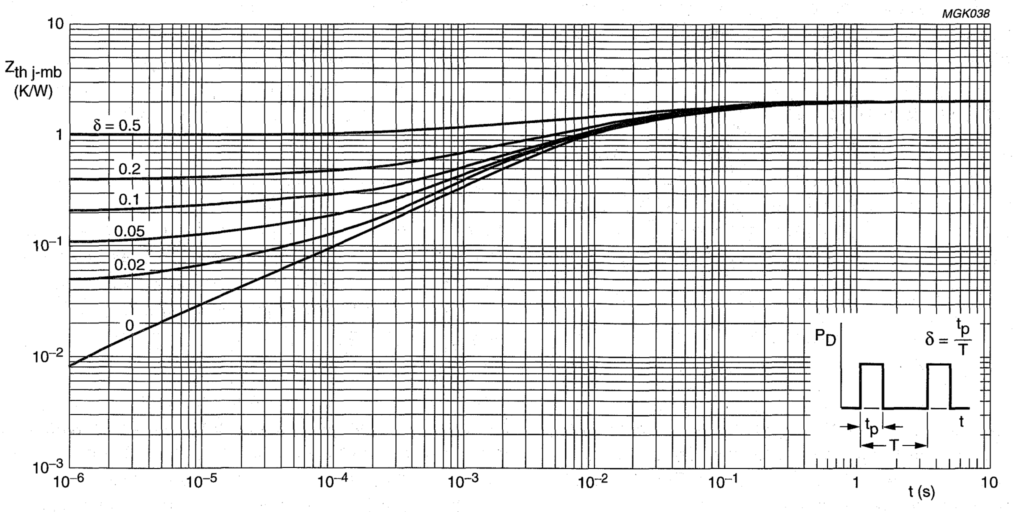


Fig.9 Examples of the transient thermal impedance as a function of the pulse time with duty factor as parameter.

In general, the shorter the pulse and the lower the frequency, the lower the temperature that the junction reaches. By analogy with Equation (3), it follows that:

$$P_{tot\ M} = \frac{T_j - T_{mb}}{Z_{thj-mb}} \qquad (5)$$

where $Z_{thj\text{-}mb}$ is the transient thermal impedance between the junction and mounting base of the device. It depends on the pulse duration t_p, and the duty factor δ, where:

$$\delta = \frac{t_p}{T} \qquad (6)$$

and T is the pulse period. Figure 9 shows a typical family of curves for thermal impedance against pulse duration, with duty factor as a parameter.

Again, the maximum pulse power dissipation is limited either by the maximum temperature difference $\Delta T_{j\text{-}mb\ max}$ (Equation (2)), or by the maximum junction temperature T_{jmax}, and so by analogy with Equations (3)and (4):

$$P_{tot\ max\ K} = \frac{\Delta T_{j-mbmax}}{Z_{thj-mb}} \qquad (7)$$

when $T_{mb} \le T_{mb\ K}$, and:

$$P_{tot\ M\ max} = \frac{T_{jmax} - T_{mb}}{Z_{thj-mb}} \qquad (8)$$

when $T_{mb} > T_{mb\ K}$. That is, below a mounting-base temperature of $T_{mb\ K}$, the maximum power dissipation has a fixed limit value; and above $T_{mb\ K}$, the power dissipation must be reduced linearly with increasing mounting-base temperature.

Short pulse duration (Fig.10a)

As the pulse duration becomes very short, the fluctuations of junction temperature become negligible, owing to the internal thermal capacity of the transistor. Consequently, the only factor to be considered is the heating of the junction by the average power dissipation; that is:

$$P_{tot(av)} = \delta P_{totM} \qquad (9)$$

The transient thermal impedance becomes:

$$\lim_{t_p \to 0} Z_{thj-mb} = \delta R_{thj-mb} \qquad (10)$$

The $Z_{thj\text{-}mb}$ curves approach this value asymptotically as t_p decreases. Figure 9 shows that, for duty factors in the range 0.1 to 0.5, the limit values given by Equation (10) have virtually been reached at $t_p = 10^{-6}$ s.

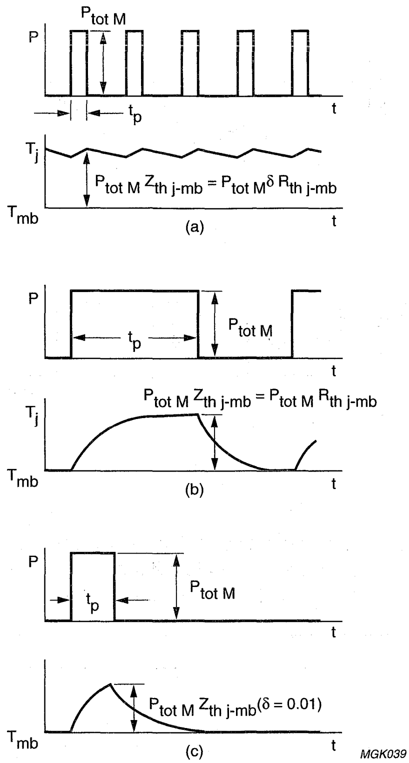


Fig.10 Three limit cases of rectangular pulse loads: (a) short pulse duration, (b) long pulse duration, (c) single-shot pulse.

Long pulse duration (Fig.10b)

As the pulse duration increases, the junction temperature approaches a stationary value towards the end of a pulse. The transient thermal impedance tends to the thermal resistance for continuous power dissipation; that is:

$$\lim_{t_p \to \infty} Z_{thj-mb} = R_{thj-mb} \qquad (11)$$

Figure 9 shows that $Z_{thj\text{-}mb}$ approaches this value as t_p becomes large. In general, transient thermal effects die out in most power transistors within 0.1 to 1.0 seconds. This time depends on the material and construction of the case, the size of the chip, the way it is mounted, and other factors. Power pulses with a duration in excess of this time have approximately the same effect as a continuous load.

Single-short pulse (Fig.10c)

As the duty factor becomes very small, the junction tends to cool down completely between pulses so that each pulse can be treated individually. When considering single pulses, the $Z_{thj\text{-}mb}$ values for $\delta = 0$ (Fig.9) give sufficiently accurate results.

PART TWO: WORKED EXAMPLES

Calculating junction temperatures

Most applications which include power semiconductors usually involve some form of pulse mode operation. This section gives several worked examples showing how junction temperatures can be simply calculated. Examples are given for a variety of waveforms:

1. periodic waveforms
2. single-shot waveforms
3. composite waveforms
4. a pulse burst
5. non-rectangular pluses.

From the point of view of reliability, it is most important to know what the peak junction temperature will be when the power waveform is applied and also what the average junction temperature is going to be.

Peak junction temperature will usually occur at the end of an applied pulse and its calculation will involve transient thermal impedance. The average junction temperature (where applicable) is calculated by working out the average power dissipation using the DC thermal resistance.

When considering the junction temperature in a device, the following formula is used:

$$T_j = T_{mb} + \Delta T_{j-mb} \tag{12}$$

where $\Delta T_{j\text{-}mb}$ is found from a rearrangement of Equation (7). In all the following examples the mounting base temperature (T_{mb}) is assumed to be 75 °C.

Periodic rectangular pulse

Figure 11 shows an example of a periodic rectangular pulse. This type of pulse is commonly found in switching applications. 100 W is dissipated every 400 µs for a period of 20 µs, representing a duty cycle (δ) of 0.05.

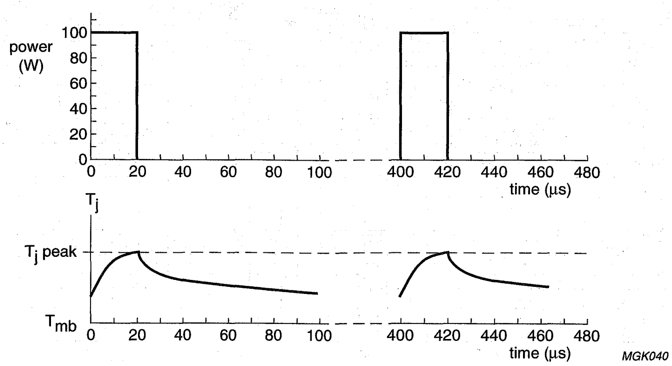


Fig.11 Periodic rectangular pulse.

The peak junction temperature is calculated as follows:

Peak T_j:

$t = 2 \times 10^{-5}$ s

$P = 100$ W

$\delta = \frac{20}{100} = 0.05$

$Z_{thj-mb} = 0.12$ K/W

$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.12 = 12\ ^{o}C$

$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 12 = 87\ ^{o}C$

Average T_j:

$P_{av} = P \times \delta = 100 \times 0.05 = 5$ W

$\Delta T_{j-mb(av)} = P_{av} \times Z_{thj-mb(\delta=1)} = 5 \times 2 = 10\ ^{o}C$

$T_{j(av)} = T_{mb} + \Delta T_{j-mb(av)} = 75 + 10 = 85\ ^{o}C$

The value for $Z_{th\ j-mb}$ is taken from the $\delta = 0.05$ curve shown in Fig.12 (This diagram repeats Fig.9 but has been simplified for clarity). The above calculation shows that the peak junction temperature will be 85 °C.

Single shot rectangular pulse

Figure 13 shows an example of a single shot rectangular pulse. The pulse used is the same as in the previous example, which should highlight the differences between periodic and single shot thermal calculations. For a single shot pulse, the time period between pulses is infinity, i.e. the duty cycle $\delta = 0$. In this example 100 W is dissipated for a period of 20 µs. To work out the peak junction temperature the following steps are used:

$t = 2 \times 10^{-5}$ s

$P = 100$ W

$\delta = 0$

$Z_{thj-mb} = 0.04$ K/W

$\Delta T_{j-mb} = P \times Z_{thj-mb} = 100 \times 0.04 = 4$ °C

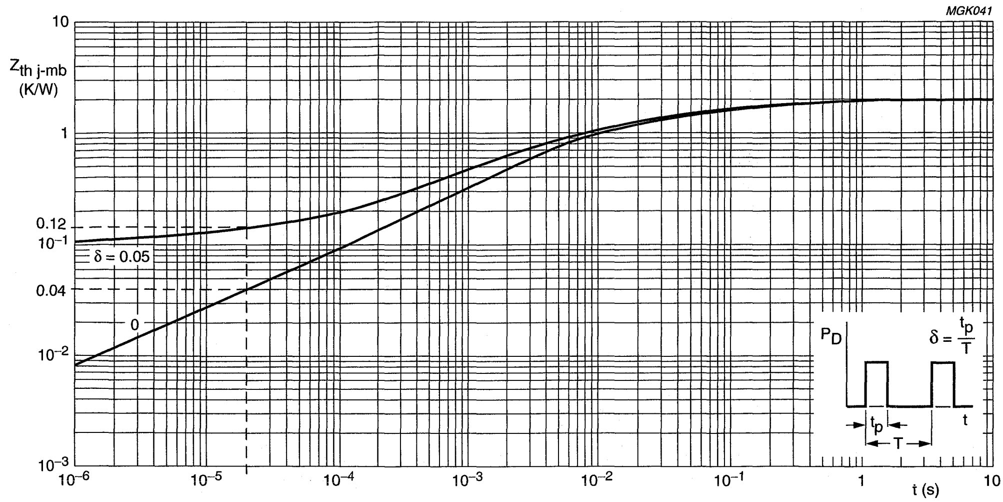


Fig.12 Thermal impedance curves for δ = 0.05 and δ = 0.

The value for $Z_{th\ j\text{-}mb}$ is taken from the $\delta = 0$ curve shown in Fig.12. The above calculation shows that the peak junction temperature will be 4 °C above the mounting base temperature.

For a single shot pulse, the average power dissipated and average junction temperature are not relevant.

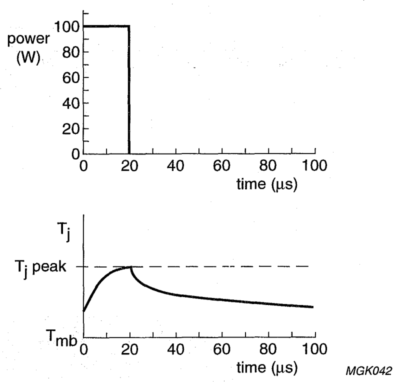


Fig.13 Single shot pulse.

Composite rectangular pulse

In practice, a power device frequently has to handle composite waveforms, rather than the simple rectangular pulses shown so far. This type of signal can be simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of t_p and δ.

By way of an example, consider the composite waveform shown in Fig.14. To show the way in which the method used for periodic rectangular pulses is extended to cover composite waveforms, the waveform shown has been chosen to be an extension of the periodic rectangular pulse example. The period is 400 µs, and the waveform consists of three rectangular pulses, namely 40 W for 10 µs, 20 W for 150 µs and 100 W for 20 µs. The peak junction temperature may be calculated at any point in the cycle. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time t_x in the first calculation and t_y in the second calculation. Positive pulses increase the junction temperature, while negative pulses decrease it.

Calculation for time t_x

$$\Delta T_{j+mb@x} = P_1 \times Z_{thj-mb(t1)} + P_2 \times Z_{thj-mb(t3)} + P_3 \times Z_{thj-mb(t4)} - P_1 \times Z_{thj-mb(t2)} - P_2 \times Z_{thj-mb(t4)} \qquad (13)$$

In Equation (15), the values for P_1, P_2 and P_3 are known: $P_1 = 40$ W, $P_2 = 20$ W and $P_3 = 100$ W. The Z_{th} values are taken from Fig.9. For each term in the equation, the equivalent duty cycle must be worked out. For instance the first superimposed pulse in Fig.14 lasts for a time $t_1 = 180$ µs, representing a duty cycle of $180/400 = 0.45 = \delta$. These values can then be used in conjunction with Fig.9 to find a value for Z_{th}, which in this case is 0.9 K/W. Table 1 gives the values calculated for this example.

Table 1 Composite pulse parameters for time t_x

		t1 180 µs	t2 170 µs	t3 150 µs	t4 20 µs
Repetitive	δ	0.450	0.425	0.375	0.050
T = 400 µs	Z_{th}	0.900	0.850	0.800	0.130
Single shot	δ	0.000	0.000	0.000	0.000
T = ∞	Z_{th}	0.130	0.125	0.120	0.040

Substituting these values into Equation (15) for $T_{j\text{-}mb@x}$ gives:

Repetitive:

$$\Delta T_{j-mb@x} = 40 \times 0.9 + 20 \times 0.85 + 100 \times 0.13 - 40 \times 0.85 - 20 \times 0.13 = 29.4\ ^\circ C$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 29.4 = 104.4\ ^\circ C$$

Single shot:

$$\Delta T_{j-mb@x} = 40 \times 0.13 + 20 \times 0.125 + 100 \times 0.04 - 40 \times 0.125 - 20 \times 0.04 = 5.9\ ^\circ C$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 5.9 = 80.9\ ^\circ C$$

Hence the peak values of T_j are 104.4 °C for the repetitive case, and 80.9 °C for the single shot case.

Thermal considerations Chapter 5

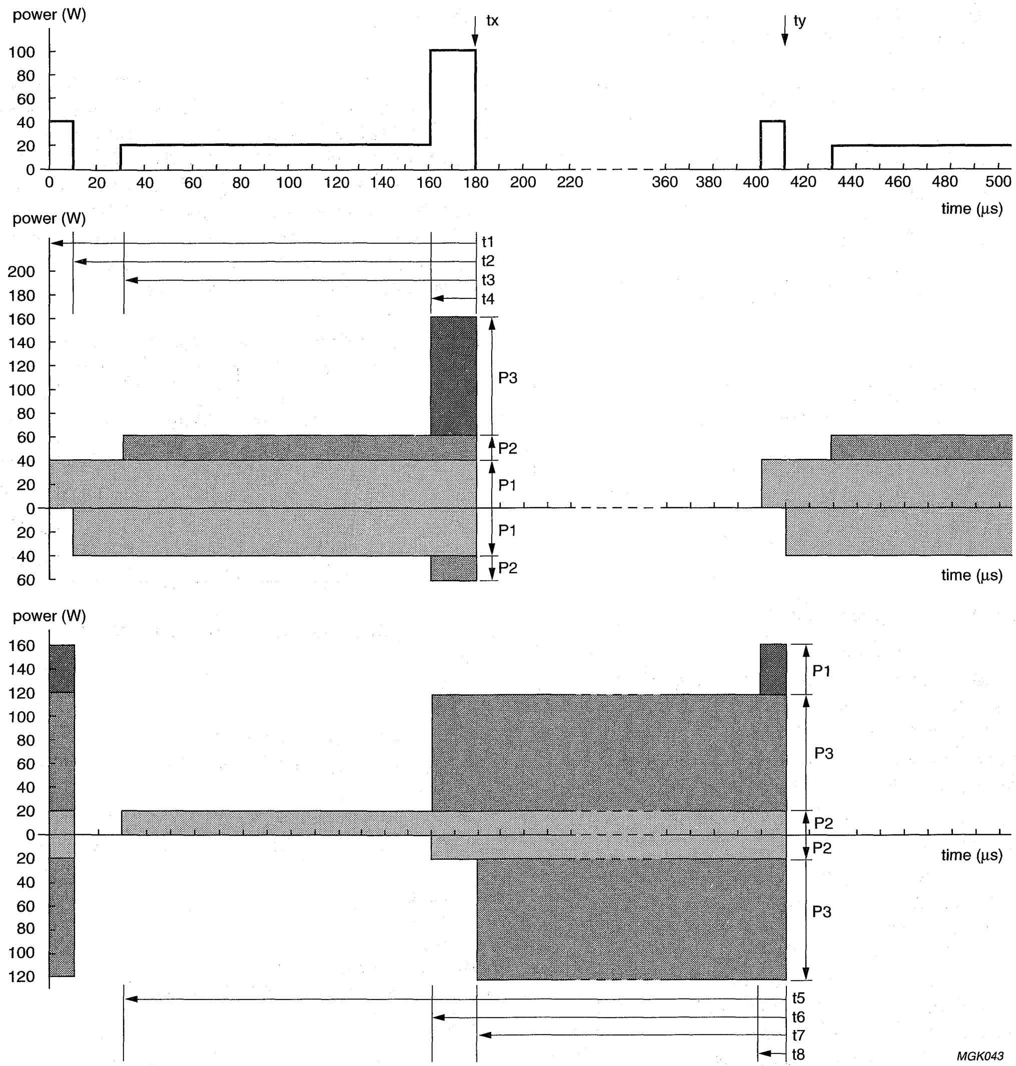


Fig.14 Periodic composite waveform.

Calculation for time t_y

$$\Delta T_{j+mb@y} = P_2 \times Z_{thj-mb(t5)} + P_3 \times Z_{thj-mb(t6)} + P_1 \times Z_{thj-mb(t8)} - P_2 \times Z_{thj-mb(t6)} - P_3 \times Z_{thj-mb(t7)} \quad (14)$$

Where $Z_{th-mb(t)}$ is the transient thermal impedance for a pulse time t.

Table 2 Composite pulse parameters for time t_y

		t5 380 µs	t6 250 µs	t7 230 µs	t8 10 µs
Repetitive	δ	0.950	0.625	0.575	0.025
T = 400 µs	Z_{th}	1.950	1.300	1.250	0.080
Single shot	δ	0.000	0.000	0.000	0.000
T = ∞	Z_{th}	0.200	0.160	0.150	0.030

Substituting these values into Equation (15) for $T_{j-mb(y)}$ gives:

Repetitive:

$$\Delta T_{j-mb(y)} = 20 \times 1.95 + 100 \times 1.3 + 40 \times 0.08 - 20 \times 1.3 - 100 \times 1.25 = 21.2\ ^{o}C$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 21.2 = 96.2\ ^{o}C$$

Single shot:

$$\Delta T_{j-mb@y} = 20 \times 0.2 + 100 \times 0.16 + 40 \times 0.03 - 20 \times 0.16 - 100 \times 0.15 = 3\ ^{o}C$$

$$T_j = T_{mb} + \Delta T_{j-mb} = 75 + 3 = 78\ ^{o}C$$

Hence the peak values of T_j are 96.2 °C for the repetitive case, and 78 °C for the single shot case.

The average power dissipation and the average junction temperature can be calculated as follows:

$$P_{av} = \frac{25 \times 10 + 5 \times 130 + 20 \times 100}{400} = 7.25\ W$$

$$\Delta T_{j-mb(av)} = P_{av} \times Z_{th-mb(\delta = 1)} = 7.25 \times 2 = 14.5\ ^{\circ}C$$

$$\Delta T_{j(av)} = T_{mb} + \Delta T_{j-mb(av)} = 75 + 14.5 = 89.5\ ^{\circ}C$$

Clearly, the junction temperature at time t_x should be higher than that at time t_y, and this is proven in the above calculations.

Burst pulses

Power devices are frequently subjected to a burst of pulses. This type of signal can be treated as a composite waveform and as in the previous example simulated by superimposing several rectangular pulses which have a common period, but both positive and negative amplitudes, in addition to suitable values of t_p and δ.

Consider the waveform shown in Fig.15. The period is 240 μs, and the burst consists of three rectangular pulses of 100 W power and 20 ms duration, separated by 30 ms. The peak junction temperature will occur at the end of each burst at time $t = t_x = 140$ μs. To be able to add the various effects of the pulses at this time, all the pulses, both positive and negative, must end at time t_x. Positive pulses increase the junction temperature, while negative pulses decrease it.

$$\Delta T_{j+mb@x} = P \times Z_{thj-mb(t1)} + P \times Z_{thj-mb(t3)} + P \times Z_{thj-mb(t5)} - P \times Z_{thj-mb(t2)} - P \times Z_{thj-mb(t4)} \quad (15)$$

where $Z_{thj\text{-}mb(t)}$ is the transient thermal impedance for a pulse time t.

The Z_{th} values are taken from Fig.9. For each term in the equation, the equivalent duty cycle must be worked out. These values can then be used in conjunction with Fig.9 to find a value for Z_{th}. Table 3 gives the values calculated for this example.

Table 3 Burst Mode pulse parameters

		t1 120 μs	t2 100 μs	t3 70 μs	t4 50 μs	t5 20 μs
Repetitive	δ	0.500	0.420	0.290	0.210	0.083
T = 240 μs	Z_{th}	1.100	0.800	0.600	0.430	0.210
Single shot	δ	0.000	0.000	0.000	0.000	0.000
T = ∞	Z_{th}	0.100	0.090	0.075	0.060	0.040

Substituting these values into Equation (17) gives:

Repetitive:

$$\Delta T_{j-mb@x} = 100 \times 1.10 + 100 \times 0.60 + 100 \times 0.21 - 100 \times 0.80 - 100 \times 0.43 = 68\ °C$$

$$T_j = 75 + 68 = 143\ °C$$

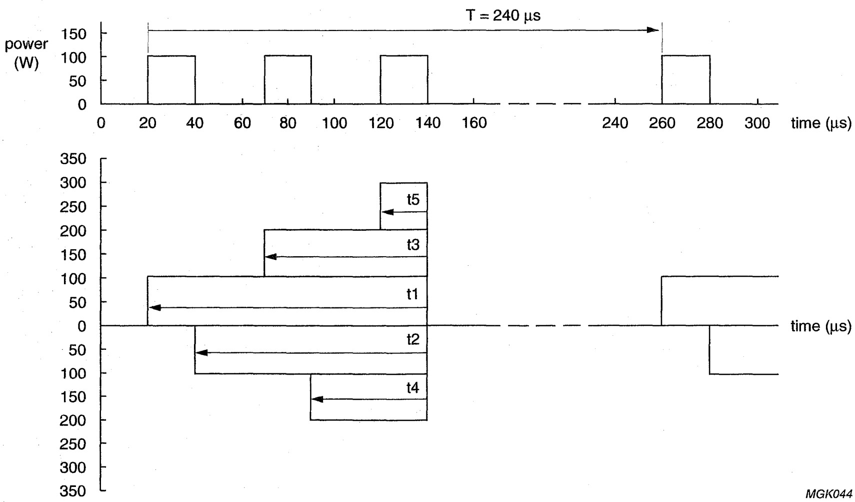


Fig.15 Burst mode waveform.

Single Shot:

$\Delta T_{j-mb@x} = 100 \times 0.10 + 100 \times 0.075$
$+ 100 \times 0.04 - 100 \times 0.09 - 100 \times 0.06$
$= 6.5\ °C$

$T_j = 75 + 6.5 = 81.5\ °C$

Hence the peak value of T_j is 143 °C for the repetitive case and 81.5 °C for the single shot case. To calculate the average junction temperature $T_{j(av)}$:

$$P_{av} = \frac{3 \times 100 \times 20}{240}$$
$$= 25\ W$$

$\Delta T_{j-mb(av)} = P_{av} \times Z_{th-mb(\delta=1)}$
$= 25 \times 2 = 50\ °C$

$\Delta T_{j(av)} = 75 + 50 = 125\ °C$

The above example for the repetitive waveform highlights a case where the average junction temperature (125 °C) is well within limits but the composite pulse calculation shows the peak junction temperature to be significantly higher. For reasons of improved long term reliability it is usual to operate devices with a peak junction temperature below 125 °C.

Non-rectangular pulses

So far, the worked examples have only covered rectangular waveforms. However, triangular, trapezoidal and sinusoidal waveforms are also common. In order to apply the above thermal calculations to non rectangular waveforms, the waveform is approximated by a series of rectangles. Each rectangle represents part of the waveform. The equivalent rectangle must be equal in area to the section of the waveform it represents (i.e. the same energy) and also be of the same peak power. With reference to Fig.16, a triangular waveform has been approximated to one rectangle in the first example, and two rectangles in the second. Obviously, increasing the number of sections the waveform is split into will improve the accuracy of the thermal calculations.

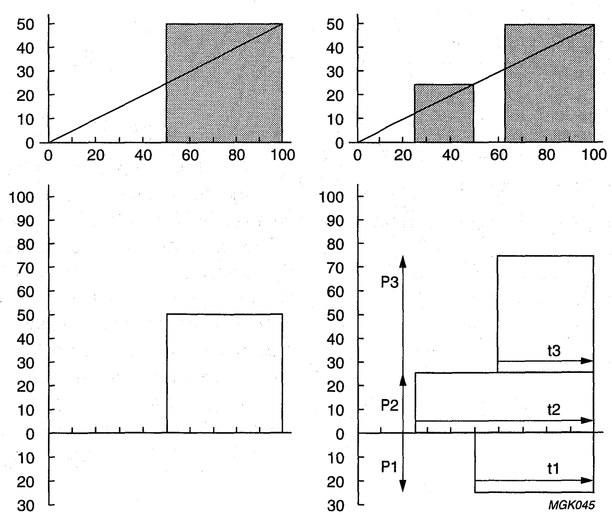


Fig.16 Non-rectangular waveform.

In the first example, there is only one rectangular pulse, of duration 50 µs, dissipating 50 W. So again using Equation (14) and a rearrangement of Equation (7):

$$\Delta T_{j-mb} = P_{tot\,M} \times Z_{thj-mb}$$

Single shot:

$$\Delta T_{j-mb} = 50 \times 0.065 = 3.25\ °C$$

$$\Delta T_{jpeak} = 75 + 3.25 = 78.5\ °C$$

10% duty cycle:

$$\Delta T_{j-mb} = 50 \times 0.230 = 11.5\ °C$$

$$\Delta T_{jpeak} = 75 + 11.5 = 86.5\ °C$$

50% duty cycle:

$$\Delta T_{j-mb} = 50 \times 1.000 = 50\ °C$$

$$\Delta T_{jpeak} = 75 + 50 = 125\ °C$$

When the waveform is split into two rectangular pulses:

$$\Delta T_{j\text{-}mb} = P_3 \times Z_{thj-mb(t3)} + P_1 \times Z_{thj-mb(t2)} - P_2 \times Z_{thj-mb(t2)} \quad (16)$$

For this example $P_1 = 25$ W, $P_2 = 25$ W, $P_3 = 50$ W. Table 4 shows the rest of the parameters.

Table 4 Non-rectangular pulse calculations

		t1 75 µs	t2 50 µs	t3 37.5 µs
Single shot	δ	0.000	0.000	0.000
T = ∞	Z_{th}	0.085	0.065	0.055
10% duty cycle	δ	0.075	0.050	0.037
T = 1000 µs	Z_{th}	0.210	0.140	0.120
50% duty cycle	δ	0.375	0.250	0.188
T = 200 µs	Z_{th}	0.700	0.500	0.420

Substituting these values into Equation (18) gives:

Single shot:

$$\Delta T_{j-mb} = 50 \times 0.055 + 25 \times 0.85 - 25 \times 0.65 = 3.25\ °C$$

$$\Delta T_{jpeak} = 75 + 3.25 = 78.5\ °C$$

10% Duty cycle

$$\Delta T_{j-mb} = 50 \times 0.12 + 25 \times 0.21 - 25 \times 0.14 = 7.75\ °C$$

$$\Delta T_{jpeak} = 75 + 7.75 = 82.5\ °C$$

50% Duty cycle

$$\Delta T_{j-mb} = 50 \times 0.42 + 25 \times 0.7 - 25 \times 0.5 = 26\ °C$$

$$\Delta T_{jpeak} = 75 + 26 = 101\ °C$$

To calculate the average junction temperature:

$$P_{av} = \frac{50 \times 50}{1000} = 2.5\ W$$

$$\Delta T_{j-mb(av)} = P_{av} \times Z_{th-mb(\delta=1)} = 2.5 \times 2 = 5\ °C$$

$$\Delta T_{j(av)} = 75 + 5 = 80\ °C$$

Conclusion to part two

A method has been presented to allow the calculation of average and peak junction temperatures for a variety of pulse types. Several worked examples have shown calculations for various common waveforms. The method for non-rectangular pulses can be applied to any wave shape, allowing temperature calculations for waveforms such as exponential and sinusoidal power pulses. For pulses such as these, care must be taken to ensure that the calculation gives the peak junction temperature, as it may not occur at the end of the pulse. In this instance several calculations must be performed with different endpoints to find the maximum junction temperature.

Thermal considerations Chapter 5

PART 3: HEAT DISSIPATION

All semiconductor failure mechanisms are temperature dependent and so the lower the junction temperature, the higher the reliability of the circuit. Thus our data specifies a maximum junction temperature which should not be exceeded under the worst probable conditions. However, derating the operating temperature from T_{jmax} is always desirable to improve the reliability still further. The junction temperature depends on both the power dissipated in the device and the thermal resistances (or impedances) associated with the device. Thus careful consideration of these thermal resistances (or impedances) allows the user to calculate the maximum power dissipation that will keep the junction temperature below a chosen value.

The formulae and diagrams given in this part can only be considered as a guide for determining the nature of a heatsink. This is because the thermal resistance of a heatsink depends on numerous parameters which cannot be predetermined. They include the position of the transistor on the heatsink, the extent to which air can flow unhindered, the ratio of the lengths of the sides of the heatsink, the screening effect of nearby components, and heating from these components. It is always advisable to check important temperatures in the finished equipment under the worst probable operating conditions. The more complex the heat dissipation conditions, the more important it becomes to carry out such checks.

Heat flow path

The heat generated in a semiconductor chip flows by various paths to the surroundings. Small signal devices do not usually require heatsinking; the heat flows from the junction to the mounting base which is in close contact with the case. Heat is then lost by the case to the surroundings by convection and radiation (Fig.17a). Power transistors, however, are usually mounted on heatsinks because of the higher power dissipation they experience. Heat flows from the transistor case to the heatsink by way of contact pressure, and the heatsink loses heat to the surroundings by convection and radiation, or by conduction to cooling water (Fig.17b). Generally air cooling is used so that the ambient referred to in Fig.17 is usually the surrounding air. Note that if this is the air inside an equipment case, the additional thermal resistance between the inside and outside of the equipment case should be taken into account.

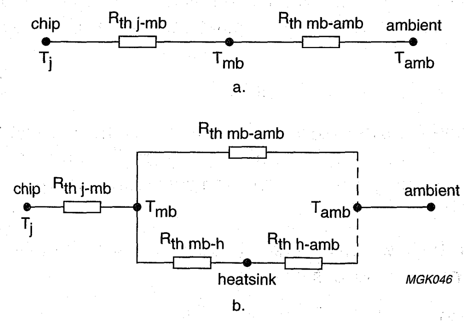


Fig.17 Thermal resistance in the heat flow process: (a) without heatsink, (b) with heatsink.

Contact thermal resistance $R_{th\ mb\text{-}h}$

The thermal resistance between the transistor mounting base and the heatsink depends on the quality and size of the contact areas, the type of any intermediate plates used, and the contact pressure. Care should be taken when drilling holes in heatsinks to avoid burring and distorting the metal, and both mating surfaces should be clean. Paint finishes of normal thickness, up to 50 µm (as a protection against electrolytic voltage corrosion), barely affect the thermal resistance. Transistor case and heatsink surfaces can never be perfectly flat, and so contact will take place on several points only, with a small air-gap over the rest of the area. The use of a soft substance to fill this gap lowers the contact thermal resistance. Normally, the gap is filled with a heatsinking compound which remains fairly viscous at normal transistor operating temperatures and has a high thermal conductivity. The use of such a compound also prevents moisture from penetrating between the contact surfaces. Proprietary heatsinking compounds are available which consist of a silicone grease loaded with some electrically insulating good thermally conducting powder such as alumina.The contact thermal resistance $R_{th\ mb\text{-}h}$ is usually small with respect to ($R_{th\ j\text{-}mb} + R_{th\ h\text{-}amb}$) when cooling is by natural convection. However, the heatsink thermal resistance $R_{th\ h\text{-}amb}$ can be very small when either forced ventilation or water cooling are used, and thus a close thermal contact between the transistor case and heatsink becomes particularly important.

Thermal resistance calculations

Fig.17a shows that, when a heatsink is not used, the total thermal resistance between junction and ambient is given by:

$$R_{th\ j\text{-}amb} = R_{th\ j\text{-}mb} + R_{th\ mb\text{-}amb} \quad (17)$$

However, power transistors are generally mounted on a heatsink since $R_{th\ j\text{-}amb}$ is not usually small enough to maintain temperatures within the chip below desired levels.

Fig.17b shows that, when a heatsink is used, the total thermal resistance is given by:

$$R_{th\ j\text{-}amb} = R_{th\ j\text{-}mb} + R_{th\ mb\text{-}h} + R_{th\ h\text{-}amb} \quad (18)$$

Note that the direct heat loss from the transistor case to the surroundings through $R_{th\ mb\text{-}amb}$ is negligibly small.

The first stage in determining the size and nature of the required heatsink is to calculate the maximum heatsink thermal resistance $R_{th\ h\text{-}amb}$ that will maintain the junction temperature below the desired value.

Continuous operation

Under DC conditions, the maximum heatsink thermal resistance can be calculated directly from the maximum desired junction temperature.

$$R_{th\ j\text{-}amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} \quad (19)$$

and

$$R_{th\ j\text{-}mb} = \frac{T_j - T_{mb}}{P_{tot(av)}} \quad (20)$$

Combining Equations (18) and (19) gives:

$$R_{th\ h\text{-}amb} = \frac{T_j - T_{amb}}{P_{tot(av)}} - R_{th\ j\text{-}mb} - R_{th\ mb\text{-}h} \quad (21)$$

and substituting Equation (20) into Equation (21) gives:

$$R_{th\ h\text{-}amb} = \frac{T_{mb} - T_{amb}}{P_{tot(av)}} - R_{th\ mb\text{-}h} \quad (22)$$

The values of $R_{th\ j\text{-}mb}$ and $R_{th\ mb\text{-}h}$ are given in the published data. Thus, either Equation (21) or Equation (22) can be used to find the maximum heatsink thermal resistance.

Intermittent operation

The thermal equivalent circuits of Fig.17 are inappropriate for intermittent operation, and the thermal impedance $Z_{th\ j\text{-}mb}$ should be considered.

$$P_{totM} = \frac{T_j - T_{mb}}{Z_{th\ j\text{-}mb}}$$

thus:

$$T_{mb} = T_j - P_{totM} \times Z_{th\ j\text{-}mb} \quad (23)$$

The mounting-base temperature has always been assumed to remain constant under intermittent operation. This assumption is known to be valid in practice provided that the pulse time is less than about one second. The mounting-base temperature does not change significantly under these conditions as indicated in Fig.18. This is because heatsinks have a high thermal capacity and thus a high thermal time-constant.

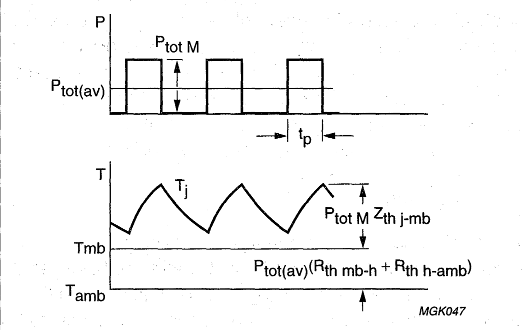


Fig.18 Variation of junction and mounting base temperature when the pulse time is small compared with the thermal time-constant of the heatsink.

Thus Equation (22) is valid for intermittent operation, provided that the pulse time is less than one second. The value of T_{mb} can be calculated from Equation (23), and the heatsink thermal resistance can be obtained from Equation (22).

The thermal time constant of a transistor is defined as that time at which the junction temperature has reached 70% of its final value after being subjected to a constant power dissipation at a constant mounting base temperature.

Now, if the pulse duration t_p exceeds one second, the transistor is temporarily in thermal equilibrium since such a pulse duration is significantly greater than the thermal time-constant of most transistors. Consequently, for pulse times of more than one second, the temperature difference $T_j - T_{mb}$ reaches a stationary final value (Fig.19) and Equation (23) should be replaced by:

$$T_{mb} = T_j - P_{totM} \times R_{th\ j\text{-}mb} \quad (24)$$

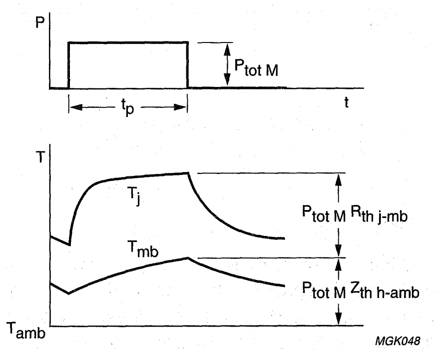


Fig.19 Variation of junction and mounting base temperature when the pulse time is not small compared with he thermal time-constant of the heatsink.

In addition, it is no longer valid to assume that the mounting base temperature is constant since the pulse time is also no longer small with respect to the thermal time constant of the heatsink.

Smaller heatsinks for intermittent operation

In many instances, the thermal capacity of a heatsink can be utilized to design a smaller heatsink for intermittent operation than would be necessary for the same level of continuous power dissipation. The average power dissipation in Equation (22) is replaced by the peak power dissipation to obtain the value of the thermal impedance between the heatsink and the surroundings.

$$Z_{th\ h\text{-}amb} = \frac{T_{mb} - T_{amb}}{P_{totM}} - R_{th\ mb\text{-}h} \quad (25)$$

The value of $Z_{th\ h\text{-}amb}$ will be less than the comparable thermal resistance and thus a smaller heatsink can be designed than that obtained using the too large value calculated from Equation (22).

Heatsinks

Three varieties of heatsink are in common use: flat plates (including chassis), diecast finned heatsinks, and extruded finned heatsinks. The material normally used for heatsink construction is aluminium although copper may be used with advantage for flat-sheet heatsinks. Small finned clips are sometimes used to improve the dissipation of low-power transistors.

Heatsink finish

Heatsink thermal resistance is a function of surface finish. A painted surface will have a greater emissivity than a bright unpainted one. The effect is most marked with flat plate heatsinks, where about one third of the heat is dissipated by radiation. The colour of the paint used is relatively unimportant, and the thermal resistance of a flat plate heatsink painted gloss white will be only about 3% higher than that of the same heatsink painted matt black. With finned heatsinks, painting is less effective since heat radiated from most fins will fall on adjacent fins but it is still worthwhile. Both anodising and etching will decrease the thermal resistivity. Metallic type paints, such as aluminium paint, have the lowest emissivities, although they are approximately ten times better than a bright aluminium metal finish.

Flat-plate heatsinks

The simplest type of heatsink is a flat metal plate to which the transistor is attached. Such heatsinks are used both in the form of separate plates and as the equipment chassis itself. The thermal resistance obtained depends on the thickness, area and orientation of the plate, as well as on the finish and power dissipated. A plate mounted horizontally will have about twice the thermal resistance of a vertically mounted plate. This is particularly important where the equipment chassis itself is used as the heatsink. In Fig.20, the thermal resistance of a blackened heatsink is plotted against surface area (one side) with power dissipation as a parameter. The graph is accurate to within 25% for nearly square plates, where the ratio of the lengths of the sides is less than 1.25:1.

Thermal considerations

Chapter 5

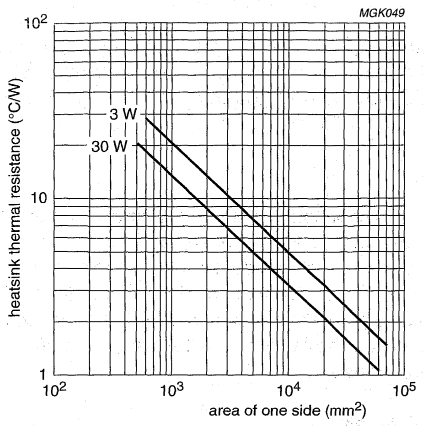


Fig.20 Generalized heatsink characteristics: flat vertical black aluminium, 3 mm thick, approximately square.

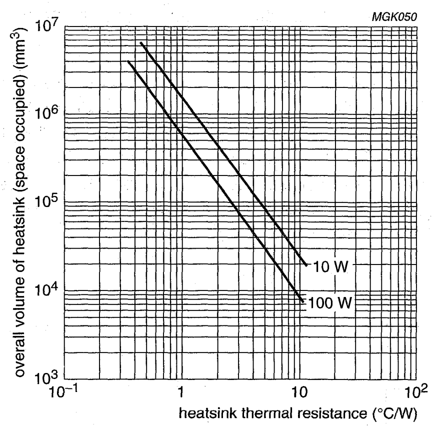


Fig.21 Generalized heatsink characteristics: blackened aluminium finned heatsinks.

Finned heatsinks

Finned heatsinks may be made by stacking flat plates, although it is usually more economical to use ready made diecast or extruded heatsinks. Since most commercially available finned heatsinks are of reasonably optimum design, it is possible to compare them on the basis of the overall volume which they occupy. This comparison is made in Fig.21 for heatsinks with their fins mounted vertically; again, the graph is accurate to 25%.

Heatsink dimensions

The maximum thermal resistance through which sufficient power can be dissipated without damaging the transistor can be calculated as discussed previously. This section explains how to arrive at a type and size of heatsink that gives a sufficiently low thermal resistance.

Natural air cooling

The required size of aluminium heatsinks - whether flat or extruded (finned) can be derived from the nomogram in Fig.22. Like all heatsink diagrams, the nomogram does not give exact values for $R_{th\ h\text{-}amb}$ as a function of the dimensions since the practical conditions always deviate to some extent from those under which the nomogram was drawn up. The actual values for the heatsink thermal resistance may differ by up to 10% from the nomogram values. Consequently, it is advisable to take temperature measurements in the finished equipment, particularly where the thermal conditions are critical.

Thermal considerations Chapter 5

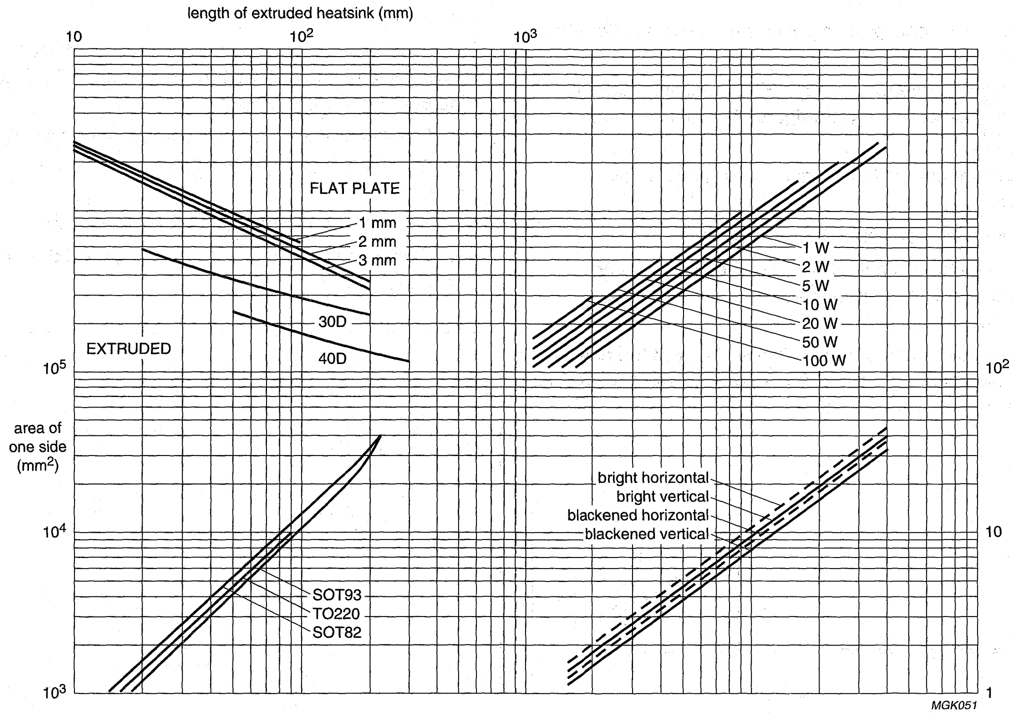


Fig.22 Heatsink nomogram.

Thermal considerations Chapter 5

The conditions to which the nomogram applies are as follows:

- natural air cooling (unimpeded natural convection with no build up of heat)
- ambient temperature about 25 °C, measured about 50 mm below the lower edge of the heatsink (see Fig.23)
- single mounting (that is, not affected by nearby heatsinks)
- atmospheric pressure about 10 N/m^2
- distance between the bottom of the heatsink and the base of a draught-free space about 100 mm (see Fig.23)
- transistor mounted roughly in the centre of the heatsink (this is not so important for finned heatsinks because of the good thermal conduction).

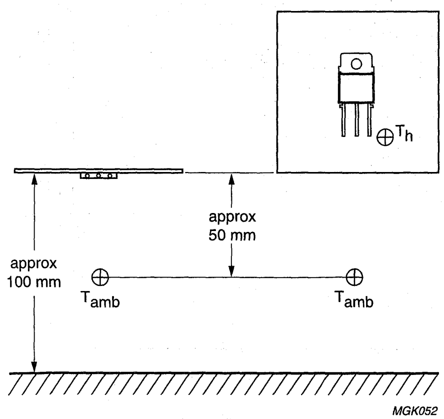


Fig.23 Conditions applicable to nomogram shown in Fig.22.

The appropriately-sized heatsink is found as follows.

1. Enter the nomogram from the right hand side of section 1 at the appropriate $R_{th\ h\text{-}amb}$ value (see Fig.24). Move horizontally to the left, until the appropriate curve for orientation and surface finish is reached.
2. Move vertically upwards to intersect the appropriate power dissipation curve in section 2.
3. Move horizontally to the left into section 3 for the desired thickness of a flat-plate heatsink, or the type of extrusion.
4. If an extruded heatsink is required, move vertically upwards to obtain its length (Figs 25a and 25b give the outlines of the extrusions).
5. If a flat-plate heatsink is to be used, move vertically downwards to intersect the appropriate curve for envelope type in section 4.
6. Move horizontally to the left to obtain heatsink area.
7. The heatsink dimensions should not exceed the ratio of 1.25:1.

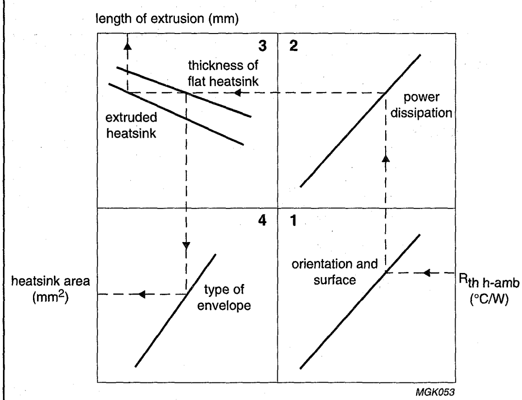


Fig.24 Use of the heatsink nomogram.

Thermal considerations Chapter 5

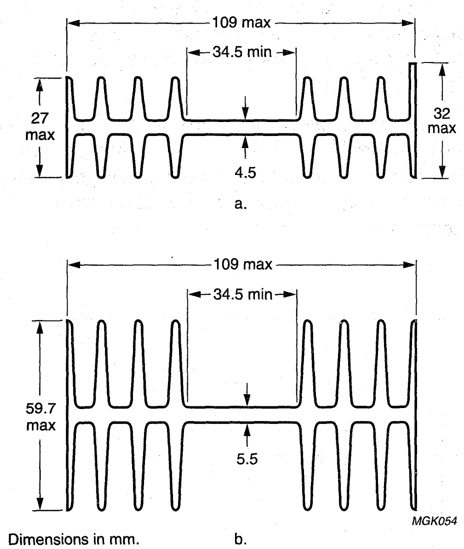


Fig.25 Outline of extrusion: a = 30D, b = 40D.

The curves in section 2 take account of the non linear nature of the relationship between the temperature drop across the heatsink and the power dissipation loss. Thus, at a constant value of the heatsink thermal resistance, the greater the power dissipation, the smaller is the required size of heatsink. This is illustrated by the following example.

Example

An extruded heatsink mounted vertically and with a painted surface is required to have a maximum thermal resistance of $R_{th\ h\text{-}amb}$ = 2.6 °C/W at the following powers:

a) $P_{tot\ (av)}$ = 5 W

b) $P_{tot\ (av)}$ = 50 W

Enter the nomogram at the appropriate value of the thermal resistance in section 1, and via either the 50 W or 5 W line in section 2, the appropriate lengths of the extruded heatsink 30D are found to be:

a) length = 110 mm

b) length = 44 mm

Case (b) requires a shorter length since the temperature difference is ten times greater than in case (a).

As the ambient temperature increases beyond 25 °C, so does the temperature of the heatsink and thus the thermal resistance (at constant power) decreases owing to the increasing role of radiation in the heat removal process. Consequently, a heatsink with dimensions derived from Fig.22 at T_{amb} > 25 °C will be more than adequate. If the maximum ambient temperature is less than 25 °C, then the thermal resistance will increase slightly. However, any increase will lie within the limits of accuracy of the nomogram and within the limits set by other uncertainties associated with heatsink calculations.

For heatsinks with relatively small areas, a considerable part of the heat is dissipated from the transistor case. This is why the curves in section 4 tend to flatten out with decreasing heatsink area. The area of extruded heatsinks is always large with respect to the surface of the transistor case, even when the length is small.

If several transistors are mounted on a common heatsink, each transistor should be associated with a particular section of the heatsink (either an area or length according to type) whose maximum thermal resistance is calculated from Equations (21) or (22); that is, without taking the heat produced by nearby transistors into account. From the sum of these areas or lengths, the size of the common heatsink can then be obtained. If a flat heatsink is used, the transistors are best arranged as shown in Fig.26. The maximum mounting base temperatures of transistors in such a grouping should always be checked once the equipment has been constructed.

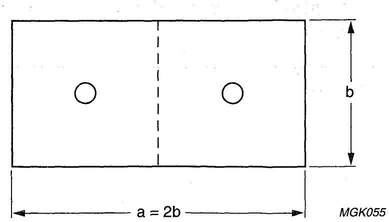


Fig.26 Arrangement of two equally loaded transistors mounted on a common heatsink.

Forced air cooling

If the thermal resistance needs to be much less than 1 °C/W, or the heatsink not too large, forced air cooling by means of fans can be provided. Apart from the size of the heatsink, the thermal resistance now only depends on the speed of the cooling air. Provided that the cooling air flows parallel to the fins and with sufficient speed (>0.5 m/s), the thermal resistance hardly depends on the power dissipation and the orientation of the heatsink. Note that turbulence in the air current can result in practical values deviating from theoretical values.

Figure 27 shows the form in which the thermal resistances for forced air cooling are given in the case of extruded heatsinks. It also shows the reduction in thermal resistance or length of heatsink which may be obtained with forced air cooling.

The effect of forced air cooling in the case of flat heatsinks is seen from Fig.28. Here, too, the dissipated power and the orientation of the heatsink have only a slight effect on the thermal resistance, provided that the air flow is sufficiently fast.

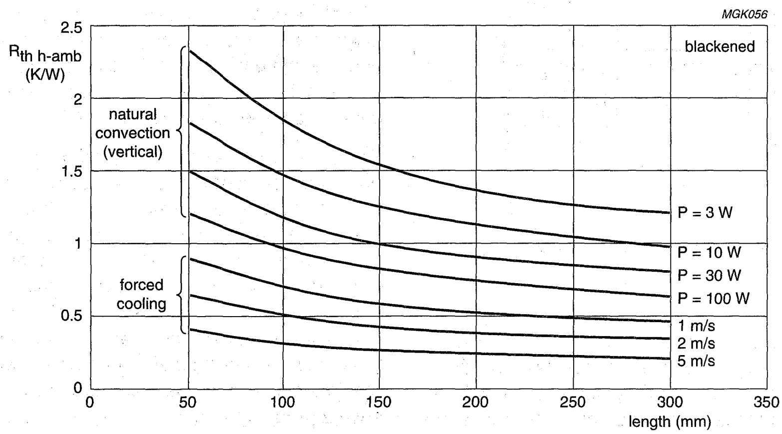
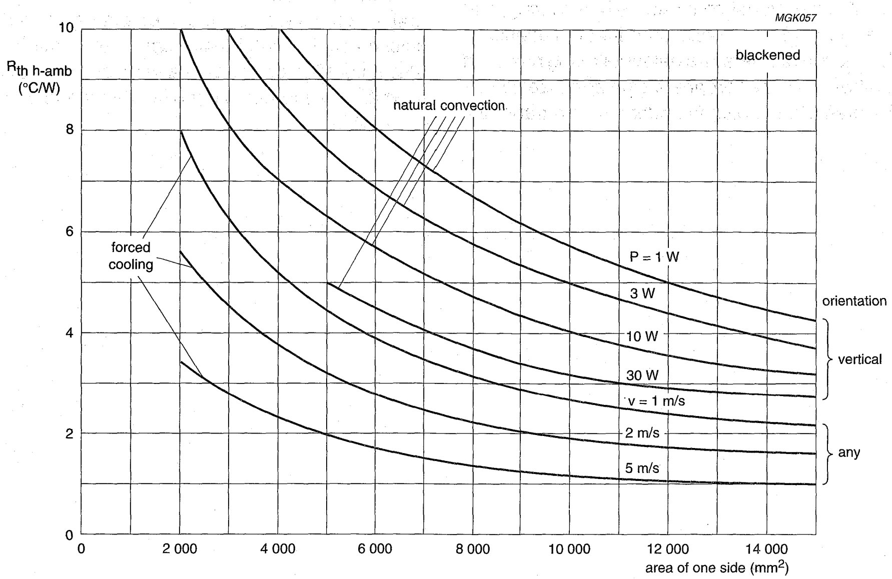


Fig.27 Thermal resistance of a finned heatsink (type 40D) as a function of the length, with natural and forced air cooling.

Thermal considerations

Chapter 5



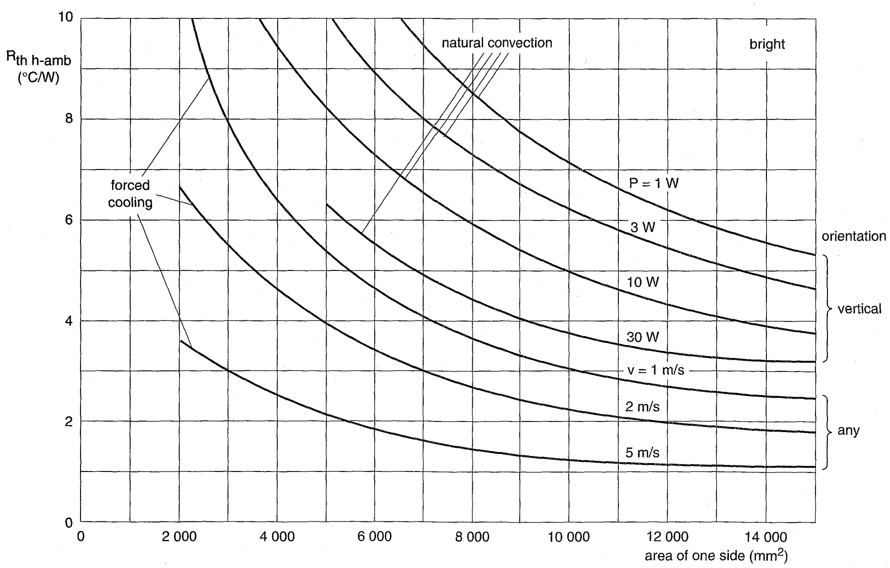


Fig.28 Thermal resistance of heatsinks (2 mm thick copper or 3 mm aluminium) under natural convection and forced cooling conditions, with a SOT93 package.

Conclusion to part three

The majority of power transistors require heatsinking, and when the maximum thermal resistance that will maintain the device's junction temperature below its rating has been calculated, a heatsink of appropriate type and size can be chosen. The practical conditions under which a transistor will be operated are likely to differ from the theoretical considerations used to determine the required heatsink, and so temperatures should always be checked in the finished equipment. Finally, some applications require a small heatsink, or one with a very low thermal resistance, in which case forced air cooling by means of fans should be provided.

CHAPTER 6

PACKING METHODS

Packing Methods Chapter 6

INTRODUCTION

This chapter contains a survey of some of the packing methods most frequently used by Philips Semiconductors. It includes information that may be important to customers when making their purchasing decisions, for example the main dimensions, shapes, and packing quantities.

Standardization

For semiconductors, packing serves two important functions. The first and most obvious function is protection during storage and transport to customers. This, of course, applies to all products, not just semiconductors. The second is to act as a delivery medium for automatic placement machines during equipment manufacture. To do this effectively, the reels, trays and tubes that components are packed in must meet recognized standards. In this respect, Philips Semiconductors actively cooperates with standardization authorities throughout the world.

In addition, our packing methods meet all major international standards, including those of IEC (International Electrotechnical Commission), JEDEC (Joint Electron Device Engineering Council, USA) and NEDA (National Electronic Distributor Association, USA).

Environmental care

Nowadays, an important issue is environmental impact. Component and equipment manufacturers are continuously working to improve the environment friendliness of their products and packing, and have devoted much effort to eliminating the use of toxic materials and to looking at ways in which materials can be recycled.

In these respects, Philips Semiconductors has taken several important steps on the packing front. These include:

- Reducing the amount of packing material by switching to 'one piece' boxes (instead of boxes with upper and lower parts)
- Changing to 'mono material' to aid recycling. For example, from aluminium-lined boxes to carbon-coated boxes.
- Changing from white boxes to natural brown boxes to eliminate the use of bleach (chlorine) in their manufacture.

The aim is minimum waste and minimum environmental impact. We have already gone a long way towards this in the development of our packing methods. And future developments will take us even further along this route.

For more information on environmental issues, refer to Chapter 7: Environmental information.

More Information

For more information about packing methods, please contact:

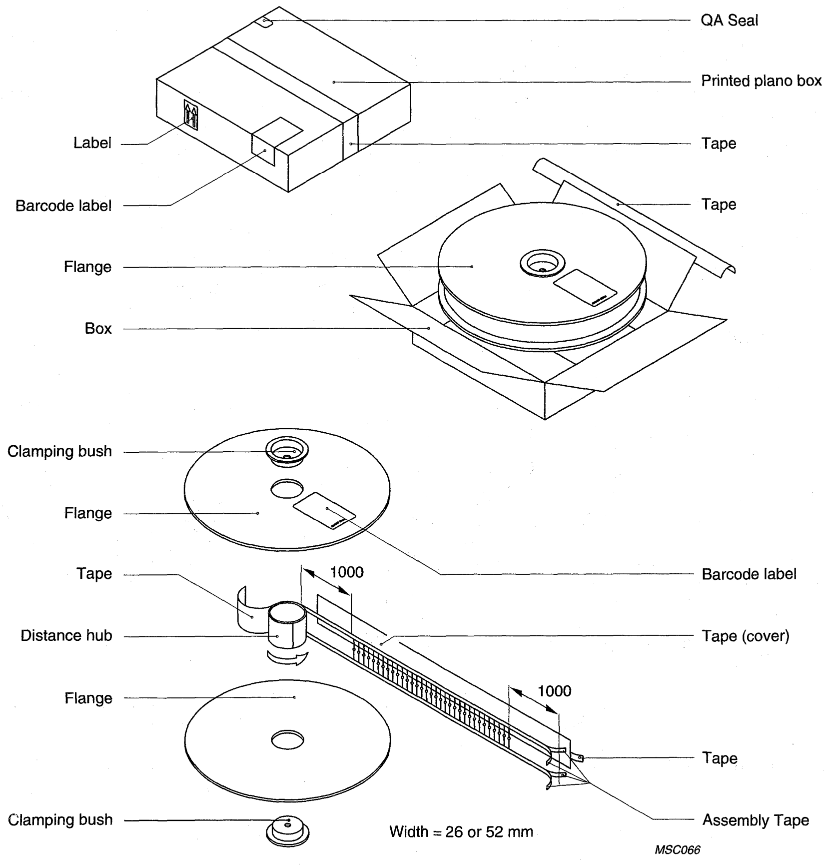
Philips Semiconductors Packing Management,
BAE-09
P.O. Box 218,
5600 MD Eindhoven
The Netherlands.

GLOSSARY OF TERMS

Carrier	Plastic tube, tray or tape with cavities, which can contain IC products
Package	Container with leads for an IC chip (also known as an envelope or outline)
Packing method	Combination of a carrier and a box to protect products during transport and storage
Pin	Rigid plastic pin that closes a tube for DIP packages by insertion through holes in its end
Plug	Flexible plastic plug that closes a tube for PLCC or SIL packages by insertion into its end
PQ	Packing Quantity, in a box containing one or more SPQs
SOD	Standard Outline Diode
SOT	Standard Outline Transistor
SPQ	Smallest Packing Quantity, mostly the quantity in one carrier
Surface mount	Mounted on the surface of a PCB
Through-hole	Mounted onto a PCB by insertion of leads into holes
Turnlock	Rigid plastic pin that closes a tube for SO packages by insertion into its end and turning to lock in place

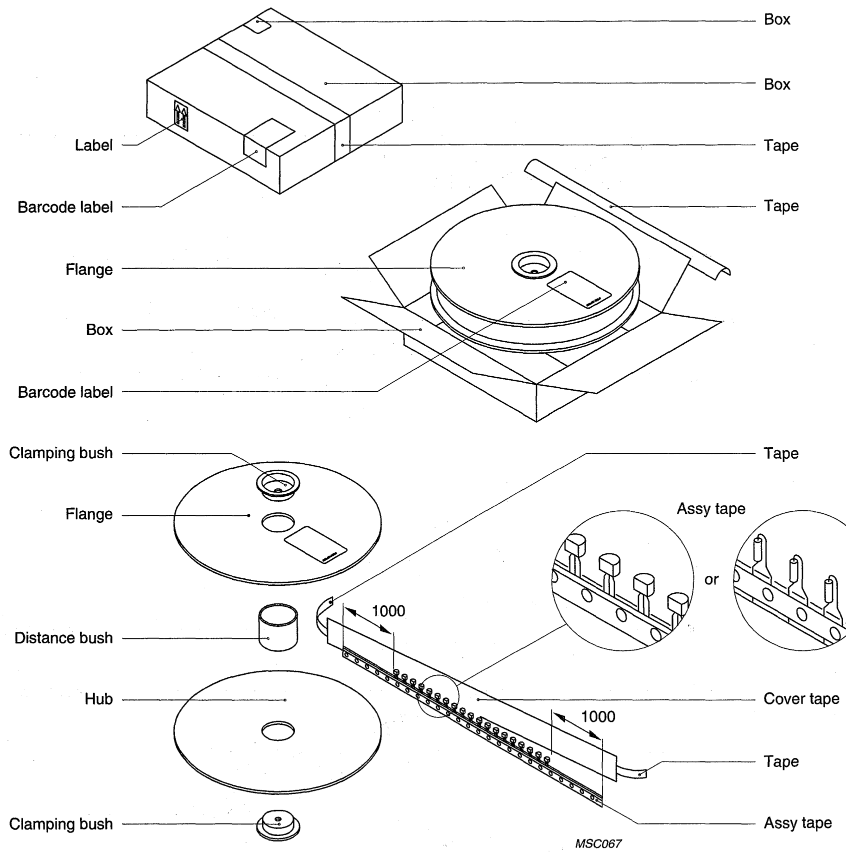
Packing Methods Chapter 6

PACKING METHODS IN EXPLODED VIEW



Dimensions in mm.

Fig.1 Reel pack axial taped.



Dimensions in mm.

Fig.2 Reel pack radial taped.

Packing Methods Chapter 6

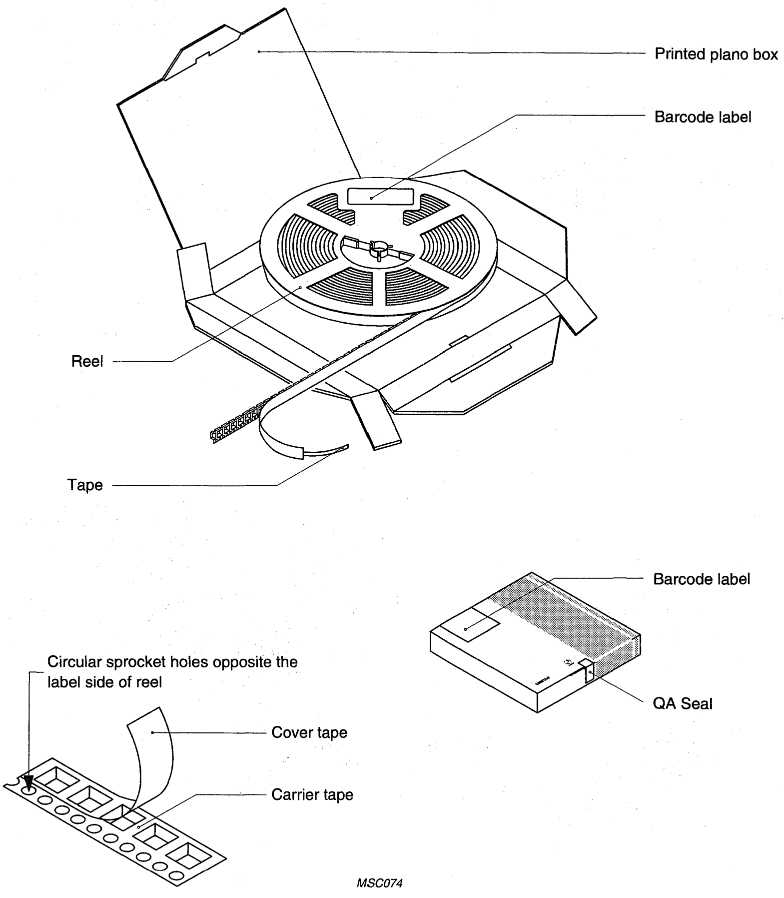


Fig.3 Reel pack for SMD.

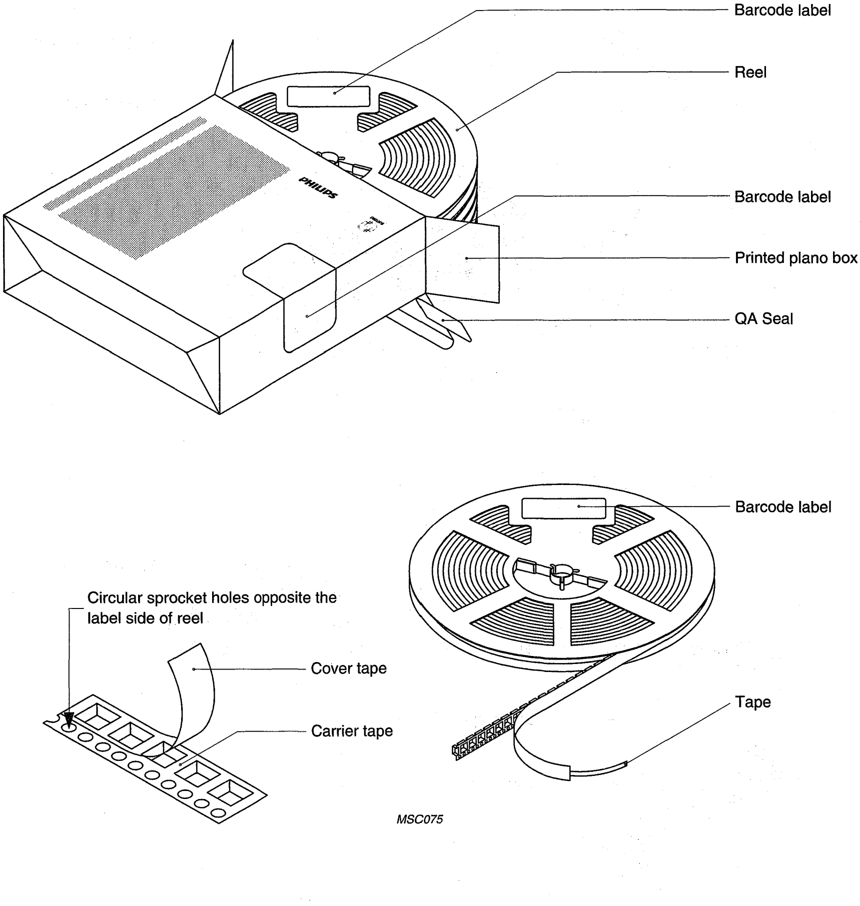


Fig.4 Five reel pack for SMD.

Packing Methods — Chapter 6

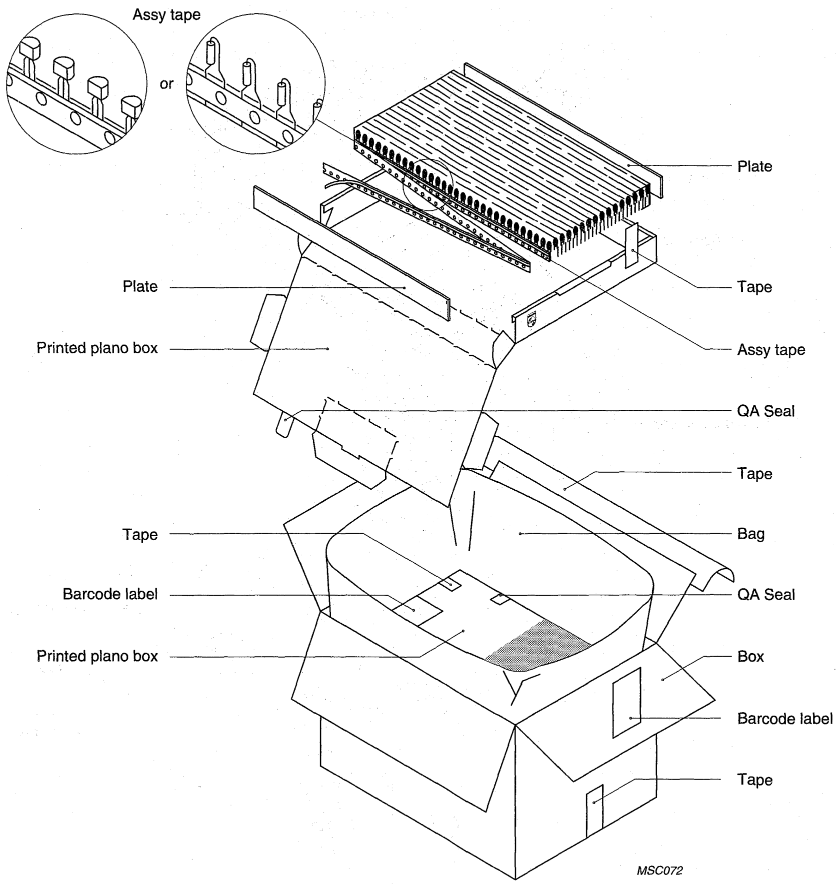


Fig.5 Five ammo pack radial taped.

Packing Methods

Chapter 6

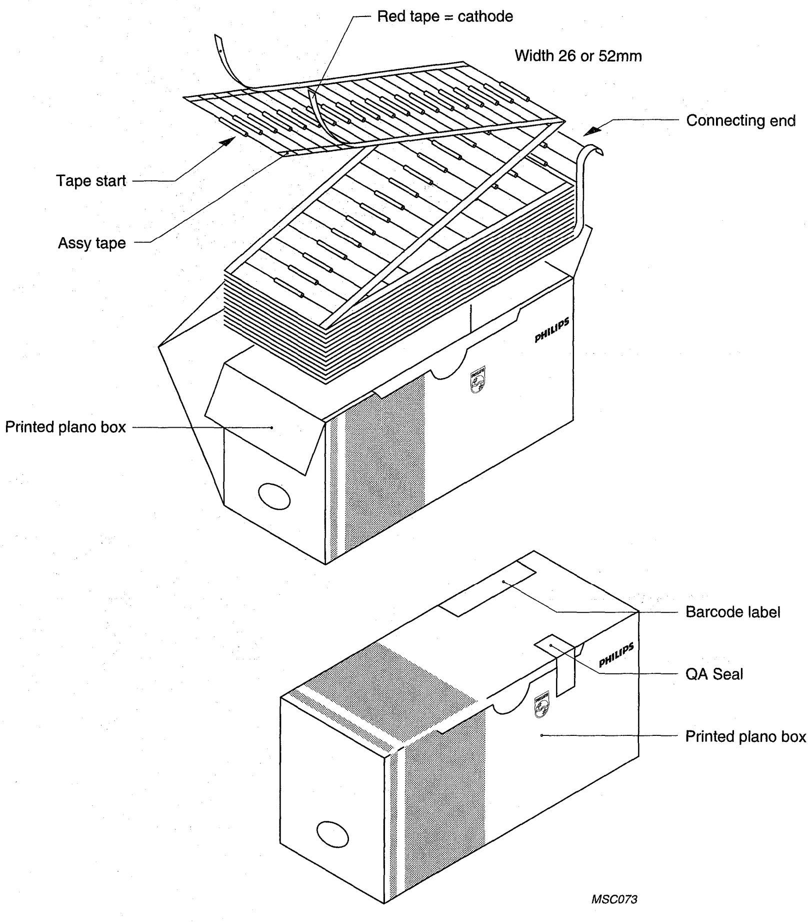


Fig.6 Ammo pack axial taped.

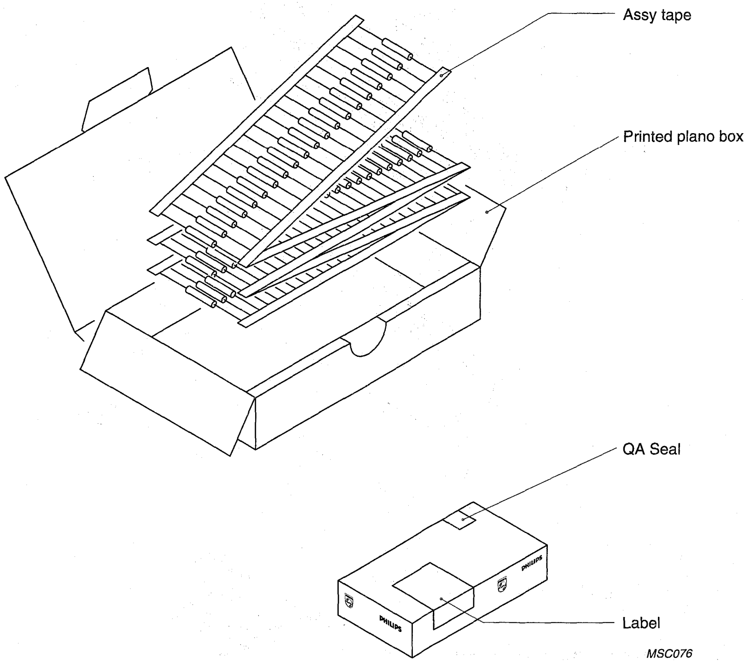


Fig.7 Ammo pack axial taped small size.

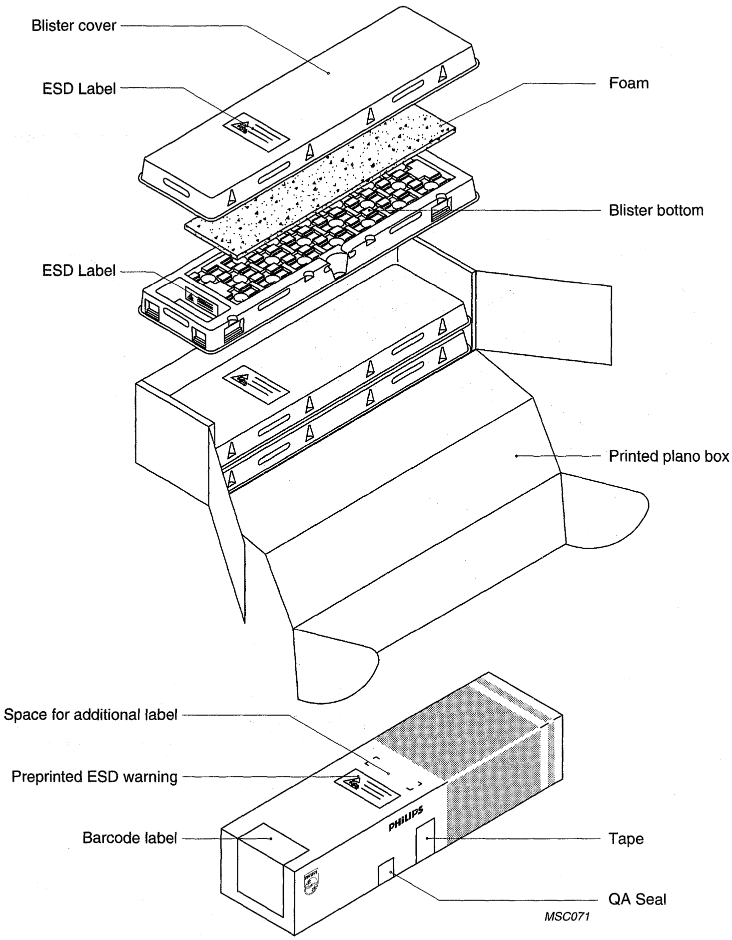


Fig.8 Blister pack.

Packing Methods Chapter 6

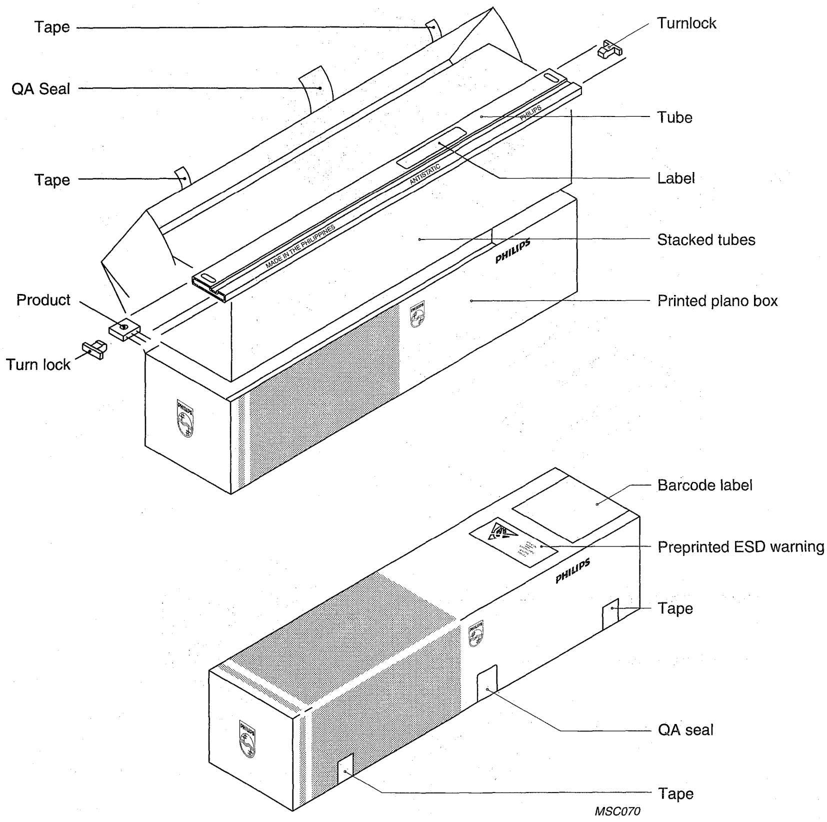


Fig.9 Tube pack.

Packing Methods Chapter 6

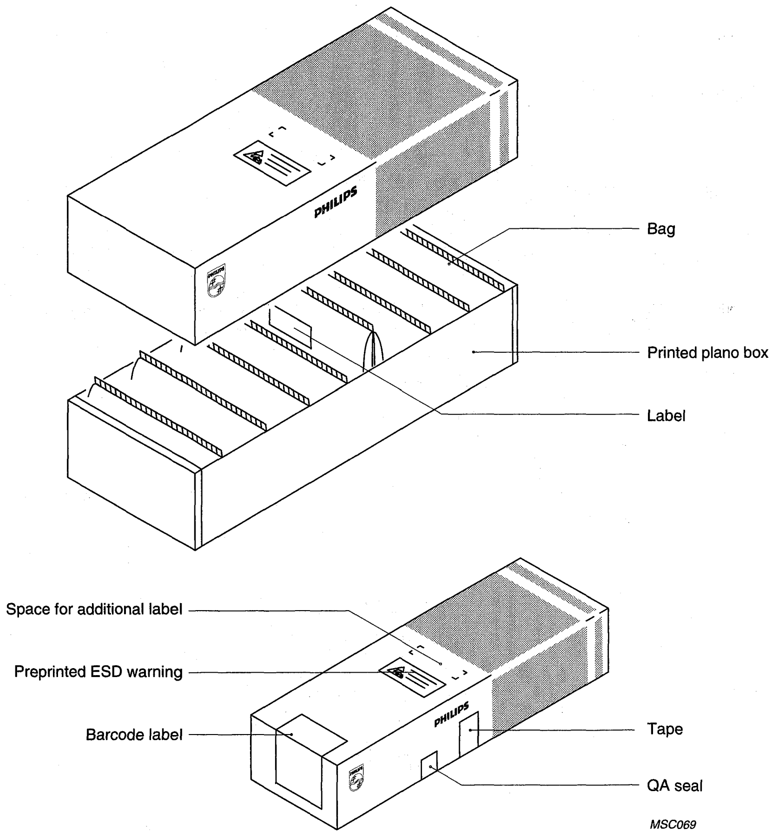


Fig.10 Bulk pack (bag).

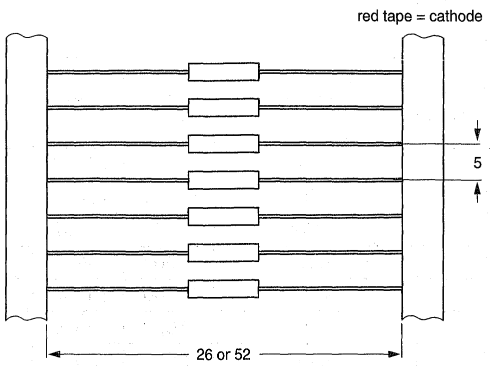
Packing Methods | Chapter 6

PACKING QUANTITIES, BOX DIMENSIONS AND CARRIER SHAPES

Reel pack - axial and radial taped

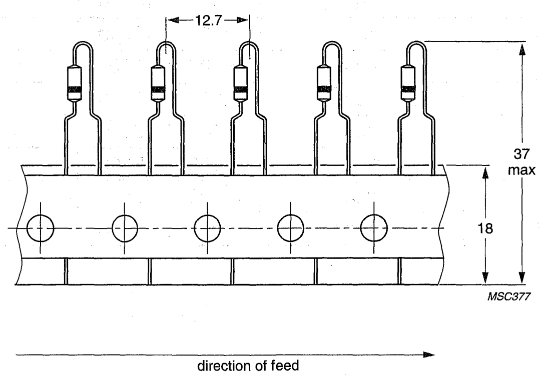
PHILIPS PACKAGE TYPE/OUTLINE CODE	TAPPING WIDTH (mm)	METHOD	SPQ	PQ	OUTER BOX DIMENSIONS L × W × H (mm)
SOD27	26	axial	10000	10000	358 × 358 × 56
	52	axial	10000	10000	356 × 356 × 88
	37	radial	5000	5000	360 × 360 × 60
SOD57	52	axial	5000	5000	356 × 356 × 88
	52	axial	10000	10000	356 × 356 × 88
SOD61	52	axial	5000	5000	356 × 356 × 102
SOD64	52	axial	5000	5000	356 × 356 × 88
SOD66	52	axial	5000	5000	356 × 356 × 88
SOD68	26	axial	10000	10000	358 × 358 × 56
	52	axial	10000	10000	356 × 356 × 88
SOD70	32	radial	2000	10000	385 × 385 × 275
SOD81	52	axial	5000	5000	356 × 356 × 88
SOD83	52	axial	2000	2000	356 × 356 × 102
SOD88	52	axial	5000	5000	356 × 356 × 102
SOD89	52	axial	2000	2000	356 × 356 × 102
SOD91	52	axial	10000	10000	356 × 356 × 88
SOT54	32	radial	2000	10000	395 × 395 × 290

Packing Methods



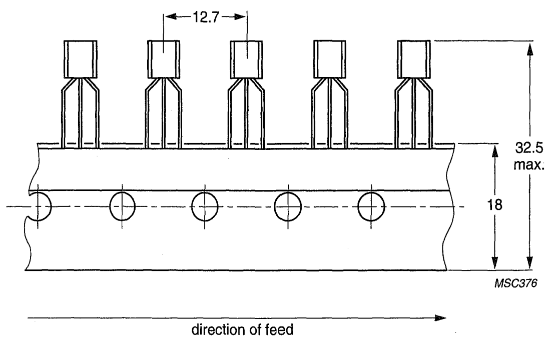
Dimensions in mm.

Fig.11 Axial taped components for reel pack.



Dimensions in mm.

Fig.12 Radial taped components for reel pack.



Dimensions in mm.

Fig.13 Radial taped components for reel pack.

Packing Methods Chapter 6

Tape and reel - surface mount devices

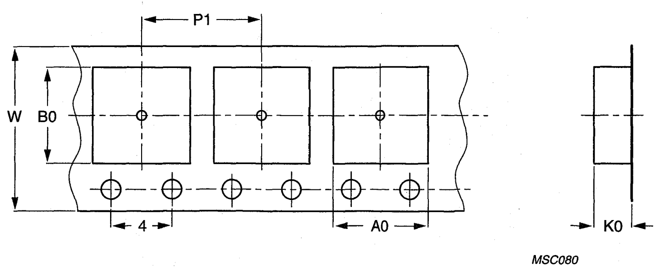
PHILIPS PACKAGE TYPE/OUTLINE CODE	REEL DIMENSIONS D × W (mm)	SPQ AND PQ	REELS PER BOX	OUTER BOX DIMENSIONS L × W × H (mm)
SOD80	180 × 8	2500	1	186 × 186 × 16
	330 × 8	10000	1	338 × 338 × 18
	330 × 8	50000	5	339 × 339 × 71
SOD87	180 × 8	2000	1	186 × 186 × 16
	180 × 8	10000	5	182 × 182 × 55
	330 × 8	8000	1	338 × 338 × 18
	330 × 8	40000	5	339 × 339 × 71
SOD106	180 × 12	1500	1	186 × 186 × 24
SOD110	180 × 8	3000	1	186 × 186 × 16
	330 × 8	10000	1	338 × 338 × 18
SOD323	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOD523	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT23	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT89	180 × 12	1000	1	186 × 186 × 24
	330 × 12	4000	1	338 × 338 × 24
SOT96-1 (SO8)	180 × 12	1000	1	190 × 190 × 26
	330 × 12	2500	1	340 × 340 × 26
SOT143	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT163-1 (SO20)	180 × 24	500	1	190 × 190 × 38
	330 × 24	2000	1	340 × 340 × 38
SOT223	180 × 12	1000	1	186 × 186 × 24
	330 × 12	4000	1	338 × 338 × 24
SOT323	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT343	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT346	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT353	180 × 8	3000	1	186 × 186 × 16
SOT363	180 × 8	3000	1	186 × 186 × 16
SOT404	330 × 24	800	1	340 × 340 × 38
SOT409	180 × 16	500	1	186 × 186 × 30
SOT416	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18

PHILIPS PACKAGE TYPE/OUTLINE CODE	REEL DIMENSIONS D × W (mm)	SPQ AND PQ	REELS PER BOX	OUTER BOX DIMENSIONS L × W × H (mm)
SOT426	330 × 24	800	1	340 × 340 × 38
SOT428	330 × 16	2500	1	340 × 340 × 30
SOT453A	330 × 32	1300	1	340 × 340 × 49
SOT453B	330 × 32	600	1	340 × 340 × 49
SOT453C	330 × 32	800	1	340 × 340 × 49
SOT457	180 × 8	3000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18
SOT482	330 × 24	2000	1	340 × 340 × 38
SOT490	180 × 8	4000	1	186 × 186 × 16
	286 × 8	10000	1	293 × 293 × 18

Tape and reel - carrier tape dimensions

PHILIPS PACKAGE TYPE/OUTLINE CODE	**CARRIER TAPE DIMENSIONS (mm)** (See Figs. 15 and 14)				
	A0	B0	K0	P1	W
SOD80	1.6	3.9	1.7	4.0	8.0
SOD87	2.0	3.9	2.3	4.0	8.0
SOD106	3.1	5.6	2.7	4.0	12.0
SOD110	1.6	2.3	1.6	4.0	8.0
SOD323	1.6	2.9	1.2	4.0	8.0
SOD523	0.9	1.4	1.0	4.0	8.0
SOT23	3.1	2.6	1.3	4.0	8.0
SOT89	4.3	4.6	1.6	8.0	12.0
SOT96-1 (SO8)	6.7	5.4	1.8	8.0	12.0
SOT143	3.1	2.6	1.3	4.0	8.0
SOT163-1 (SO20)	11.1	13.5	2.7	12.0	24.0
SOT223	7.0	7.4	1.9	8.0	12.0
SOT323	2.4	2.4	1.2	4.0	8.0
SOT343	2.4	2.4	1.2	4.0	8.0
SOT346	3.1	3.2	1.3	4.0	8.0
SOT353	2.4	2.4	1.2	4.0	8.0
SOT363	2.4	2.4	1.2	4.0	8.0
SOT404	10.6	15.8	4.9	16.0	24.0
SOT409	6.0	8.0	2.5	8.0	16.0
SOT416	1.9	1.8	1.0	4.0	8.0
SOT426	10.6	15.8	4.9	16.0	24.0
SOT428	7.0	10.5	2.5	8.0	16.0
SOT453A	10.2	21.8	2.8	16.0	32.0
SOT453B	11.1	21.8	6.6	16.0	32.0
SOT453C	10.0	20.5	4.8	16.0	32.0

PHILIPS PACKAGE TYPE/OUTLINE CODE	**CARRIER TAPE DIMENSIONS (mm)** (See Figs. 15 and 14)				
	A0	**B0**	**K0**	**P1**	**W**
SOT457	3.2	3.2	1.2	4.0	8.0
SOT482A/C	8.3	13.8	2.3	12.0	24.0
SOT490	1.9	1.8	0.9	4.0	8.0



Dimensions in mm.

Fig.14 Carrier tape for surface mount devices.

Packing Methods

Chapter 6

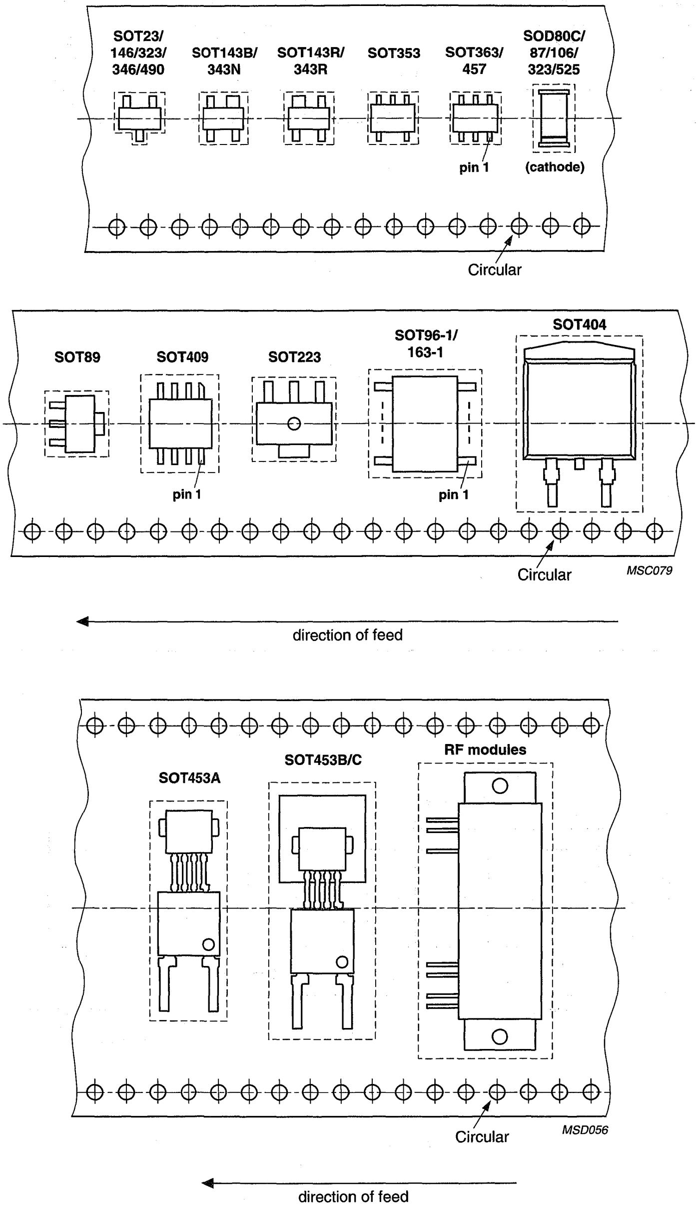
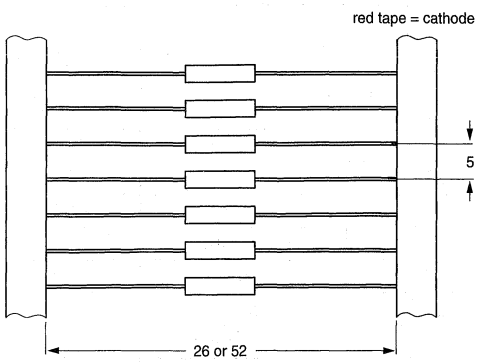


Fig.15 Product orientation in carrier tape.

Packing Methods Chapter 6

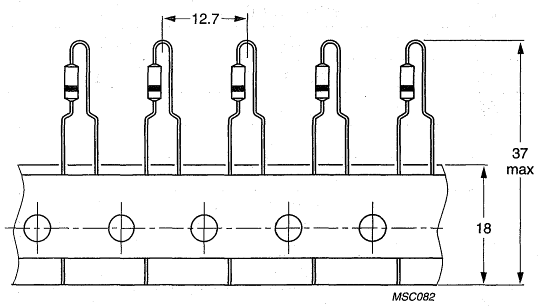
Ammo pack - axial and radial taped

PHILIPS PACKAGE TYPE/OUTLINE CODE	TAPING WIDTH (mm)	TAPING METHOD	SPQ/PQ	OUTER BOX DIMENSIONS L × W × H (mm)
SOD27	26	axial	5000	263 × 48 × 75
	52	axial/small	1000	138 × 73 × 29
	52	axial	10000	263 × 74 × 124
	37	radial	5000	350 × 203 × 42
SOD57	52	axial/small	200	138 × 73 × 29
	52	axial	2500	263 × 73 × 87
SOD61	52	axial	500	305 × 118 × 65
	52	axial/small	50	138 × 73 × 29
SOD64	52	axial	2500	263 × 73 × 87
	52	axial/small	200	138 × 73 × 29
SOD66	52	axial	5000	263 × 73 × 122
	52	axial/small	1000	138 × 73 × 29
SOD68	26	axial	5000	263 × 48 × 75
	52	axial/small	1000	138 × 73 × 29
	52	axial	10000	263 × 73 × 124
	37	radial	5000	350 × 203 × 42
	52	axial/small	500	138 × 73 × 29
SOD70	37	radial	10000	355 × 210 × 300
SOD81	26	axial	5000	255 × 50 × 89
	52	axial	5000	263 × 73 × 87
	52	axial/small	500	138 × 73 × 29
SOD91	52	axial/small	1000	138 × 73 × 29
	52	axial	2000	263 × 73 × 102
	26	axial	5000	263 × 48 × 75
	52	axial	10000	253 × 74 × 124



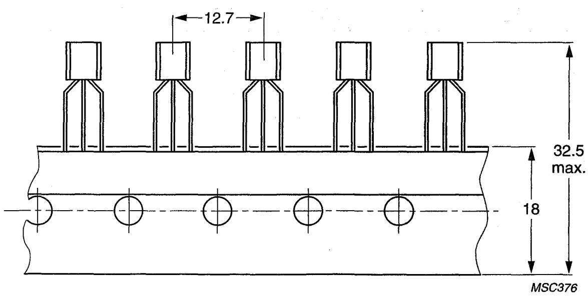
Dimensions in mm.

Fig.16 Axial taped components for ammo pack.



Dimensions in mm.

Fig.17 Radial taped components for ammo pack.



Dimensions in mm.

Fig.18 Radial taped components for ammo pack.

Blister pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER CARRIER	CARRIER PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	PACKING VERSION (See Fig.19)
SOT115	25	4	100	315 × 118 × 78	B
	5	1	5	145 × 100 × 29	C
SOT119	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT120	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT121	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT122	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT123	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT160	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT161	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT171	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT172	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT233	15	5	75	315 × 118 × 78	A
SOT262	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT268	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT273	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT279	20	2	40	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT289	20	2	40	315 × 118 × 78	B
	20	3	60	315 × 118 × 78	A
	4	8	32	315 × 118 × 78	D
SOT324	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT347	16	3	48	315 × 118 × 78	B
SOT365	15	5	75	315 × 118 × 78	A
SOT390	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER CARRIER	CARRIER PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	PACKING VERSION (See Fig.19)
SOT391	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
SOT409	25	8	200	315 × 118 × 78	D
SOT422	4	8	32	315 × 118 × 78	D
	20	3	60	315 × 118 × 78	A
SOT423	4	8	32	315 × 118 × 78	D
	20	3	60	315 × 118 × 78	A
SOT437	20	3	60	315 × 118 × 78	B
	4	8	32	315 × 118 × 78	D
	1	40	40	165 × 92 × 65	A
SOT439	1	40	40	165 × 92 × 65	A
SOT440	4	8	32	315 × 118 × 78	D
	1	40	40	165 × 92 × 65	A
SOT441	1	40	40	165 × 92 × 65	A
SOT443	20	3	60	315 × 118 × 78	A
	4	8	32	315 × 118 × 78	D
	1	40	40	165 × 92 × 65	A
SOT445	4	8	32	315 × 118 × 78	D
	1	40	40	165 × 92 × 65	A
SOT446	20	8	160	315 × 118 × 78	D
	1	40	40	165 × 92 × 65	A
SOT448	1	40	40	165 × 92 × 65	A
SOT468	20	3	60	315 × 118 × 78	A
SOT494	20	3	60	315 × 118 × 78	A
SOT504	20	3	60	315 × 118 × 78	B

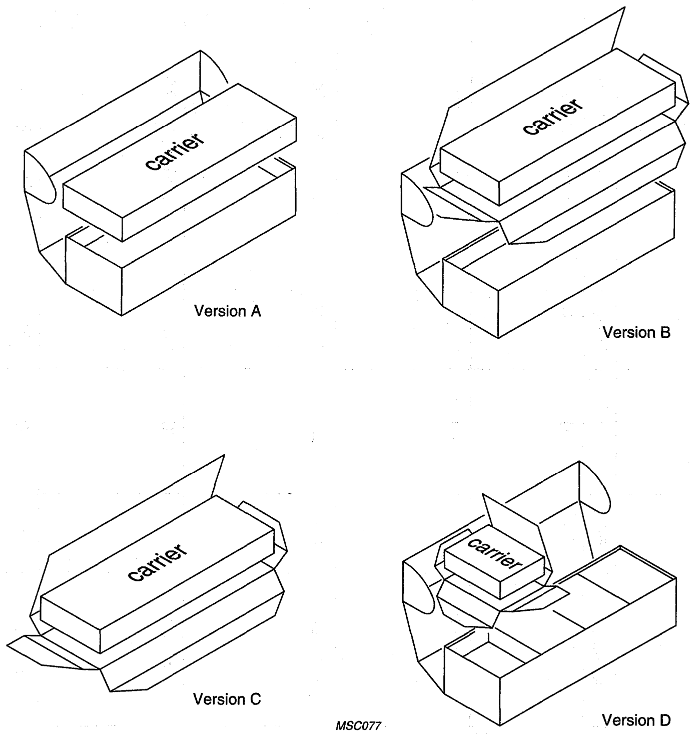
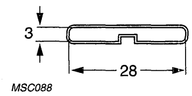
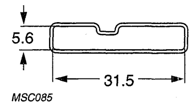
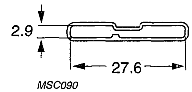
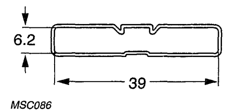
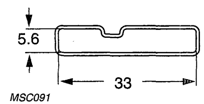
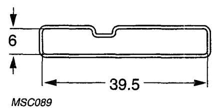


Fig.19 Packing versions of blister pack.

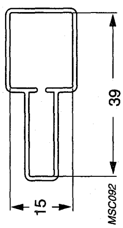
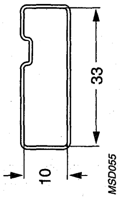
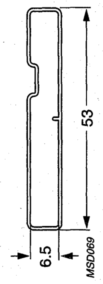
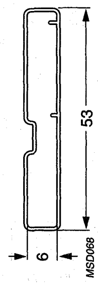
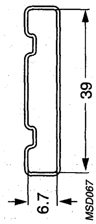
Packing Methods

Chapter 6

Tube pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	CARRIER LENGTH (mm)	END STOP	SPQ	CARRIERS PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	CARRIER PROFILE (mm)
SOT32	390	turnlock	50	20	1000	402 × 95 × 29	
SOT78	520	turnlock	50	20	1000	526 × 69 × 75	
SOT263	520	turnlock	50	20	1000	526 × 69 × 75	
SOT82	390	turnlock	50	20	1000	402 × 95 × 29	
SOT128	523	endstop	50	20	1000	529 × 84 × 85	
SOT186	520	turnlock	50	20	1000	526 × 69 × 75	
SOT199	396	turnlock	25	20	500	408 × 86 × 81	

Packing Methods

PHILIPS PACKAGE TYPE/OUTLINE CODE	CARRIER LENGTH (mm)	END STOP	SPQ	CARRIERS PER BOX	PQ	OUTER BOX DIMENSIONS L × W × H (mm)	CARRIER PROFILE (mm)
SOT199 bent lead	396	turnlock	25	12	300	408 × 86 × 81	
SOT365	413	turnlock	8	20	160	450 × 116 × 92	
SOT501A	362	turnlock	5	20	160	450 × 116 × 92	
SOT399	413	turnlock	25	20	500	450 × 116 × 92	
SOT429	413	turnlock	25	20	500	450 × 116 × 92	
SOT451A	396	turnlock	13	18	234	432 × 95 × 87	

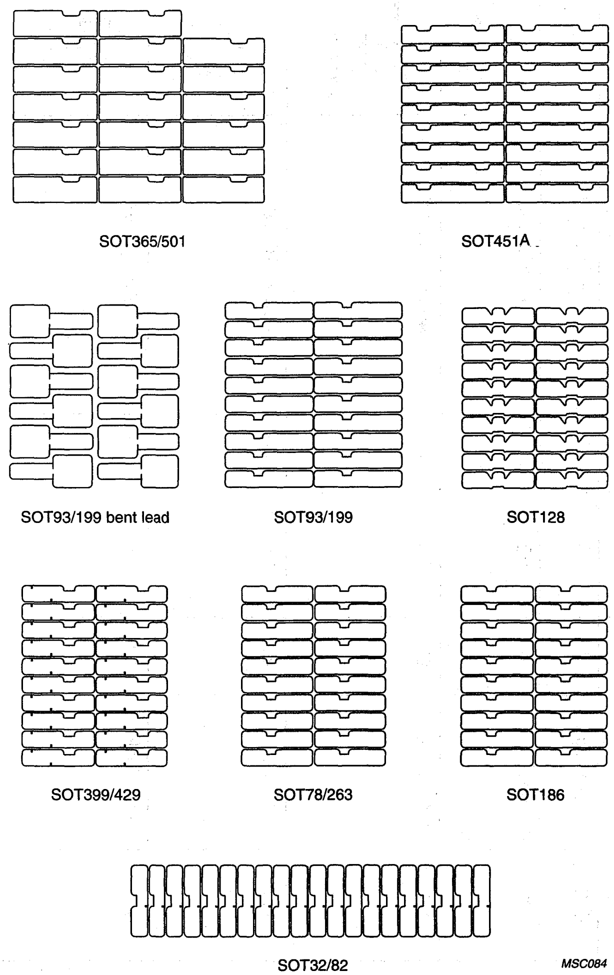


Fig.20 Stacking methods of tubes.

Bulk pack

PHILIPS PACKAGE TYPE/OUTLINE CODE	SPQ PER BAG	BAGS PER BOX	PQ	PACKING VERSION (See Fig.21)	OUTER BOX DIMENSIONS L × W × H (mm)
SOD57	100	15	1500	A	315 × 115 × 75
	250	1	250	B	138 × 73 × 30
SOD70	500	8	64000	A	305 × 120 × 67
SOD80	1000	10	10000	B	138 × 73 × 30
SOD87	1000	6	6000	B	138 × 73 × 30
SOT54	500	8	4000	A	315 × 115 × 75
SOT89	250	80	20000	A	315 × 115 × 75
SOT195	500	8	64000	A	305 × 120 × 67
SOT223	250	80	20000	A	315 × 115 × 75

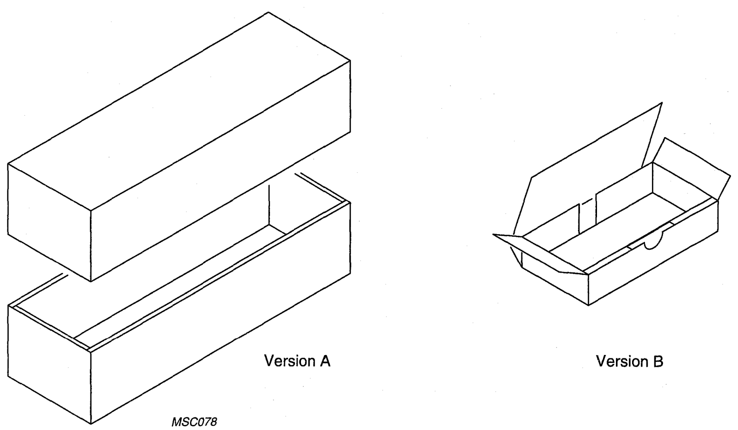


Fig.21 Bulk pack.

CHAPTER 7

ENVIRONMENTAL INFORMATION

Environmental information Chapter 7

INTRODUCTION

Nowadays, everyone must accept responsibility for keeping the environment clean, from individuals adopting a responsible attitude to their own waste disposal, however small that may be, to big industries who must take proper precautions to avoid releasing large amounts of damaging waste into the environment.

As a leading electronic components manufacturer, Philips Semiconductors has always regarded environmental protection as a major issue. The electronics industry, like many others, produces its share of toxic and hazardous materials, and we have long made it our policy to follow working practices that cut the chance of these materials passing into the environment to the absolute minimum.

Products supplied by Philips Semiconductors today offer no hazard to the environment in normal operation and when stored according to the instructions given in our data sheets. Inevitably, some products contain substances that are potentially hazardous to health if exposed by accident or misuse, but we ensure that users of these components receive clear warning of this in the data sheets. And where necessary, the warning notices contain safety precautions and disposal instructions.

This chapter supplements these notices and instructions by providing clear and comprehensive information on the composition of representative examples of discrete packages manufactured by Philips Semiconductors. This information should form a basis for answering questions on product safety and disposal and should, moreover, help to increase awareness of these aspects, not only throughout the Philips Semiconductors organization but throughout the semiconductor industry in general.

For additional information on the chemical content of discrete and IC packages, ask your local sales representative for the Philips Semiconductors brochure *Chemical content of semiconductor devices*, order number 9397 750 04906.

EXPLANATION OF THE TABLES

The following pages provide the chemical constituents of representative groups of discrete semiconductor components down to minor percentages and traces, as far as these constituents may be important to the use, destruction or disposal of the components.

The tables contain information about the materials used in the semiconductor devices themselves and in the packing used for storage, transport and assembly.

Whenever possible, the devices have been grouped into families based on the similarity in composition, construction and packing method. In this way we were able to limit the number of tables. For each group, one representative is specified in mass percentages of its parts.

In many cases, a single envelope type will contain a range of differing leadframes with different die-pad dimensions to accommodate the active devices. This, however, leads to only minor changes in the mass percentages. Different materials or techniques are sometimes used to assemble one envelope type, and whenever possible, alternative materials are included in the tables. In other cases only the standard or high-volume process is described.

Per page, the product family is defined and the types identified by the Philips package code number. Additionally, reference is made to usual names or to the JEDEC code (when applicable). The mass in milligrams (mg), body dimensions in millimeters (mm) and packing quantity are also specified.

The table itself shows the composition of the group representative broken down into the device-parts:

- metal parts
- crystal
- envelope (plastic, glass or ceramic)
- packing materials.

The device-parts are specified in milligrams (mg). These figures are as accurate as possible for the group representative shown. Other devices from the same group may differ considerably in mass. The amount of packing material, specified in grams, per device can be found by dividing the weight of the packing material by the packing quantity. For more detailed information on packing, refer to Chapter 6 Packing Methods.

Metal parts

The composition of the leadframe material is indicated, when appropriate, by the method commonly used for alloys, e.g.:

- FeNi42 means iron alloy containing 42% of nickel (alloy 42).
- CuZn15 means copper alloy containing 15% zinc (tombac).
- Cu alloy indicates copper with a small amount of alloying elements such as Fe, Ni, Zn or Ag or combinations of some elements.

Environmental information Chapter 7

Note: the die-attach material in all plastic-encapsulationed products contains on average 0.5% Au/AG, which is recoverable on recycling.

Crystal

The active device is usually a silicon chip doped with very small amounts of elements such as boron, arsenic or phosphorus. The back may be metallized with thin layers of titanium, nickel, platinum, gold or silver to enhance die-bonding to the leadframe.

Envelope

The chip is protected by a glass, ceramic, plastic or metal encapsulation. Glass will contain SiO_2 plus a number of oxides of Ba, K, Pb, Zn and Mn. These elements are, however, immobilized and will not be extracted by acids, unless the glass is ground.

The plastic encapsulation is usually based on ortho cresol novolac (OCN) -epoxy or on biphenyl-epoxy, filled with quartz particles (fused or crystalline) up to approximately 70 mass percent. In all cases (except SOT54), antimony trioxide and tetrabromobisphenol-A (TBBA) are present as flame retardants. The TBBA will be incorporated in the epoxy-polymer after curing so that no TBBA is present in the finished device. It has become a partially brominated epoxy. The flammability of all moulding compounds rates typically UL94-V0 at 1/8 inch (see page 7-5 for explanation).

Packing material

Cardboard and paper consist mainly of natural fibres. The carbon layer for ESD protection does not hamper the recyclability of the cardboard.

Polyethylene, polypropylene and polystyrene are synthetic polymers made from hydrocarbons.

Polyvinylchloride (PVC), a synthetic polymer made from chlorinated hydrocarbons, is used for the tubes in which many semiconductors are packed. PVC is hazardous to the environment when burned under certain, ill-controlled conditions. PVC is, however, readily recyclable when the material is collected separately (as a mono-material). Therefore the endpins, turnlocks and soft rubber stoppers in the PVC-tubes are now replaced by PVC to enhance recycling.

Re-use of the polystyrene (PS) reels is encouraged by requesting all our customers to return the reels after use to SemiCycle - a company set up to collect empty reels after use and sell them back to us. To facilitate this process, our reels are now manufactured as single-piece units instead of the assembled units used formally. Much lighter than earlier reels, the new reels are more economical to recycle and can be reused an average of 5 times, significantly cutting polystyrene usage.

Recycling symbols and the addresses of your nearest SemiCycle contact are printed on the boxes in which the reels are delivered.

To encourage recycling, Philips Semiconductors marks the packing materials according to ISO 11469 using the recycling symbols shown in Figs 1 to 1.

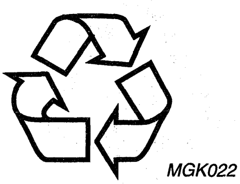


Fig.1 Paper and cardboard.

Fig.2 Polyethylene terephthalate.

Environmental information

Chapter 7

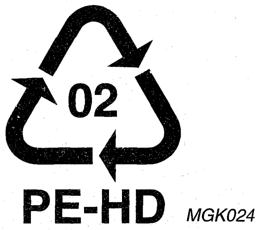


Fig.3 Polyethylene, high density.

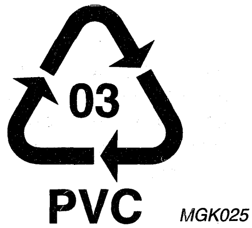


Fig.4 Polyvinylchloride.

Fig.5 Polyethylene, low density.

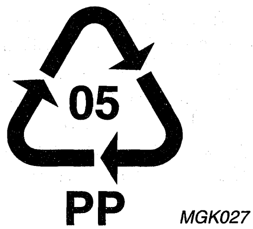


Fig.6 Polypropylene.

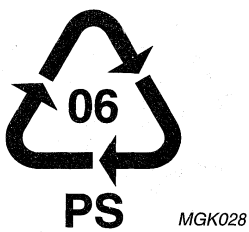


Fig.7 Polystyrene.

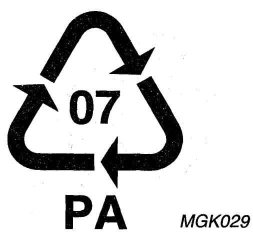


Fig.8 Other plastics. The acronym of the plastic is put under the recycling symbol. In this example: PA = polyamide.

Environmental information

Chapter 7

GENERAL SAFETY REMARKS

Oxygen index

A material's resistance to burning is expressed by its oxygen index. This is defined as the minimum concentration of oxygen, expressed as volume per cent, in a mixture of oxygen and nitrogen that will just support flaming combustion of the material initially at room temperature. All plastics used in Philips Semiconductors products are specified with an oxygen index between 28% and 35% meeting international flammability requirements

The oxygen index is measured using the standard ATSM test method designated D 2863 - 91. This test method has been found applicable for testing various forms of plastic materials, including film and cellular plastic. According to this test, the minimum concentration of oxygen that will just support combustion of the specimen in a mixture of oxygen and nitrogen flowing upward in a test column is measured under equilibrium conditions of candle-like burning. The equilibrium is established by balancing the heat lost to the surroundings with the heat generated from combustion of the specimen as measured either over a specified time of burning or length of specimen burned. The critical oxygen concentration is approached from both sides (i.e. from below and from above) to establish the oxygen index.

Beryllium oxide

Despite our constant improvement of components and processes with respect to environmental demands, some components unavoidably contain substances such as beryllium oxide that, if exposed by accident or misuse, are potentially hazardous to health. Users of the components are informed of the danger by warning notices in the data sheets supporting the components. Obviously, users of these components assume responsibility towards the consumer with respect to safety matters and environmental demands.

All used or obsolete components should be disposed of according to the regulations applying at the disposal location. Depending on the location, electronic components are considered to be 'chemical', 'special' or sometimes 'industrial' waste. Disposal as domestic waste is usually not permitted.

Underwriters Laboratories (UL)

UL is the leading third-party certification organization in the United States and the largest in North America. As a non-profit product-safety testing and certification organization, UL has been evaluating products in the interest of public safety since 1894. The organization specializes in holistic product and company evaluations, including safety, performance, energy efficiency, environmental and public health issues, electro-magnetic compatibility, quality and environmental management system registration and inspection services. It also specializes in national and international codes and standards development and harmonization.

The UL mark assures acceptance of products in North America, Europe, Asia Pacific, Asia and around the world through the most extensive network of testing, quality and certification organizations.

UL94 refers to standard "Tests for Flammability of Plastic Materials for Parts in Devices and Appliances". V0 means that the test sample complies with the highest requirements of the test.

Environmental information

SUBSTANCES NOT USED BY PHILIPS SEMICONDUCTORS

Below are listed the materials and substances that are **not** present in Philips Semiconductors' products and processes(1). This information supplements the chemical contents tables that follow and is provided to enable manufacturers assess the environmental impact of products manufactured by Philips Semiconductors.

Substances not used in products

- 4-aminodiphenyl and its salts
- ammonium salts
- arsenic
- asbestos
- benzene
- cadmium and compounds
- chlorinated paraffines
- creosote
- cyantes
- cyanides
- 4,4-diaminophenyl methane
- dibenzofurans
- epichlorhydrine
- ethylene glycol ethers
- formaldehyde
- halogenated aliphatic hydrocarbons
- hydrazine
- mercury and compounds
- N-nitrosoamines
- 2-naphthylamine and its salts
- nickel tetracarbonyl
- N,N-dimethlformamide
- N,N-dimethylacetamide
- oils and greases
- organometallic compounds (e.g. org. tin compounds)
- ozone-depleting compounds
- pentachlorophenol
- phenol compounds
- (nonyl)-phenol ethoxylates
- phtalates
- picric acid
- polybrominated biphenyl oxides (PBBO)
- polybrominated biphenyls (PBB/PBBE)
- polychlorinated triphenyls (PCT)
- polychlorinated napthalenes
- polychlorinated biphenyls (PCB)
- polycyclic compounds
- polyhalogenated dibenzofurans/dioxins
- polyhalogenated bi/triphenyl ethers
- selenium
- tellurium
- tetrabromobenzylimidazole
- tetrabromoethylene
- toluene
- triethylamine
- tris (aziridinyl) phosphinoxide
- tris (2,3-dibromopropyl) phosphate
- vinyl chloride monomer
- xylene

Substances not used in manufacturing processes

Philips Semiconductors has eliminated all Ozone Depleting Substances, referred to as Class I and II in the Montreal Protocol and its amendments. This means that our products, in compliance with the US Clean Air Act, do not have to be labelled.

We have also eliminated, voluntarily, the use of chlorinated hydrocarbons such as perchloro-ethylene and trichloro-ethylene from our manufacturing processes.

Substances not used in packing materials

- laminates with paper
- bleached paper
- polystyrene flakes (EPS)

(1) The lists refer to processes used for manufacturing products mentioned in this chapter. For information on other products, contact your sales representative.

Environmental information

Chapter 7

Summary of ozone-depleting substances eliminated

Class I substances:

- fully halogenated chloro-fluorocarbons (CFC)
- halons
- carbontetrachloride
- 1,1,1-trichloroethane

Class II substances:

- partially halogenated hydrocarbons (HCFC)

DISPOSAL AND RECYCLING

Disposal

Old or used products must be disposed of in accordance to national and local regulations.

The products and packing materials must be disposed of as special waste. This is required, in particular, for parts containing environmentally hazardous materials, for example beryllium oxide, present in some RF-devices.

Smaller quantities of material may be disposed of as domestic waste, provided national or local regulations permit this.

Recycling

Where legally required, we accept packing materials and products for recycling and/or disposal. However, since the cost of returning these materials to us must be borne by the customers, it is often more cost effective for them to look for a local recycle company. To assist in this we can provide customers with the names and addresses of local recycle companies in their areas.

In many devices, precious metals (gold and silver) are present. The content maybe 0.5% or higher.

GENERAL WARNINGS

Products

Under the specified operating conditions, no hazardous materials will be liberated from the products. The general warnings describe phenomena that can be expected with **abnormal** use (outside the product's specification). For example:

- If a product is exposed to strong acids, metals contained within it may be partially extracted.
- If a product with an epoxy moulded envelope is exposed to organic solvents, these may extract part of the resin contained in the envelope.
- If the product is incinerated, degradation and condensation reactions in the organic material it contains may cause a number of hazardous substances to be released into the air in unpredictable amounts. Moreover, metal oxides will be formed and may be released into the air as dust particles.
- If products with beryllium heatsinks (RF transistors) are damaged, toxic beryllium oxide dust may be released into the air.

Packing material

- With adequate oxygen supply, packing materials will give off mainly carbon dioxide and water if burned. However, if they are burned in a limited oxygen supply (the general case in a fire), hazardous compounds (for example carbon monoxide) may be emitted.
- PVC will form hydrochloric acid gas when incinerated. It will also generate a number of other chlorine compounds, among them the toxic dioxin, when the conditions (temperature, oxygen) are not well controlled.

Environmental information Chapter 7

GLASS DIODES/RECTIFIERS, LEADED

REFERENCE	PACKAGE CODE(1)	MASS (mg)	BODY (mm)	PACKING QUANTITY
DO-35	SOD27	136	ϕ 1.9 × 4.3	5000
DO-41	SOD66	344	ϕ 2.6 × 4.8	5000
DO-34	SOD68	118	ϕ 1.6 × 3.0	5000
IT(2)	SOD81	277	ϕ 2.2 × 3.8	5000
IT(2)	SOD91	121	ϕ 1.7 × 3.0	5000

Notes

1. All packages have a similar composition, quantities may vary.
2. IT = implosion technology.

Chemical content for group representative SOD68

DEVICE PART	SUBSTANCE	MASS (mg)
stud	FeNi42, cladded with Cu(1)	10.5
wire	Fe cladded with Cu	88
	SnPb20 plated	2.2
active device	doped Si	0.05
encapsulation	glass (Pb < 58%, Sb < 0.5%)	16.8
paint/pigment	epoxy copolymer	0.1

Note

1. Mo studs for implosion types.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	paper	53
tape	kraft paper	20
tape	polypropylene	19.6
seal	acrylate	0.2

Environmental information Chapter 7

GLASS DIODES/RECTIFIERS, SMD

REFERENCE	PACKAGE CODE[1]	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOD80	35	ϕ 1.5 × 3.5	2500
IT[2]	SOD87	50	ϕ 2.1 × 3.5	2500

Notes

1. All packages have a similar composition, quantities may vary.
2. IT = implosion technology.

Chemical content for group representative SOD87

DEVICE PART	SUBSTANCE	MASS (mg)
stud	Mo[1]	19.5
flange	Cu	15.0
	SnPb20 plated	2.5
active device	doped Si	0.4
encapsulation	glass (Pb < 54%, Sb < 0.5%)	15.5
paint/pigment	epoxy copolymer	0.1

Note

1. SOD80: FeNi42 cladded with Cu.

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	39
carrier tape	polycarbonate, carbon loaded	18.8
cover tape	polyester	3.3

Environmental information Chapter 7

GLASS-BEAD RECTIFIERS AND STACKS

REFERENCE	PACKAGE CODE[1]	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOD57	356	ϕ 3.8 × 4.6	2500
EHT-stack	SOD61	250	ϕ 3.0 × 12.5 max.[2]	5000
–	SOD64	833	ϕ 4.5 × 5.0	4000
EHT-stack	SOD83	1020	ϕ 4.5 × 12.5 max.[2]	2000
EHT-stack	SOD88	427	ϕ 3.8 × 12.5 max.[2]	5000
EHT-stack	SOD89	1196	ϕ 5.5 × 12.5 max.[2]	2000
-	SOD116	190	ϕ 2.5 × 13.5 max.	5000
-	SOD118A	178	ϕ 2.5 × 6.5	5000

Notes

1. All packages have a similar composition, quantities may vary.
2. Body length depends on reverse voltage and may be less than given here.

Chemical content for group representative SOD57

DEVICE PART	SUBSTANCE	MASS (mg)
stud	Mo	51
wire	Fe cladded with Cu	252
	SnPb20 plated	2
active device	doped Si	1[1]
encapsulation	glass (Pb < 58%[2], Sb < 0.5%)	50

Note

1. May be greater for EHT stacks.
2. In stacks Pb < 6%, ZnO = 59%.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	paper	53
reel	paper	25
tape	kraft paper	30
label	paper	0.8
seal	acrylate	0.2

DIODES IN PLASTIC PACKAGE, SMD

REFERENCE	PACKAGE CODE(1)	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOD106	66	4.7 × 2.5 × 2.6	1500
–	SOD323	4.8	1.7 × 1.3 × 0.9	3000
SC-79	SOD523	1.6	1.3 × 0.8 × 0.6	3000

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOD323

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu, SnPb20 plated	1.23
active device	doped Si	0.07
encapsulation	OCN-epoxy polymer (SiO_2 < 72%, Sb < 2%, Br < 1%)	3.5

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	74
carrier tape	polycarbonate, carbon loaded	22.6
cover tape	polyester	4
labels	paper	2.1
seal	acrylate	0.2

Environmental information

SMALL SIGNAL CERAMIC DIODE, SMD

REFERENCE	PACKAGE CODE	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOD110	10	2.0 × 1.25 × 1.45	3000

Chemical content for group representative SOD110

DEVICE PART	SUBSTANCE	MASS (mg)
envelope	Al_2O_3, SiO_2	8.2
	plated with Cu+SnPb20	1
encapsulation	OCN-epoxy polymer (SiO_2 < 70%)	0.8
active device	doped Si	< 0.1

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	56
reel	polystyrene	74
carrier tape	polycarbonate, carbon loaded	22.6
cover tape	polyester	4
labels	paper	2.1
seal	acrylate	0.2

Environmental information Chapter 7

FLANGE-MOUNTED CERAMIC RF POWER TRANSISTORS

REFERENCE	PACKAGE CODE(1)	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT119	5.20	13.0 × 25.2 × 7.5	40
–	SOT121	5.00	13.0 × 25.2 × 7.5	40
–	SOT123	3.90	9.8 × 25.2 × 7.5	40
–	SOT160	4.86	9.8 × 25.2 × 7.5	75
–	SOT161	3.50	10.2 × 25.2 × 7.5	40
–	SOT171	3.60	5.9 × 25.2 × 7.0	40
–	SOT262	8.00	10.4 × 34.3 × 5.8	16
–	SOT273	6.90	10.4 × 25.0 × 7.2	60
–	SOT289	8.20	11.8 × 28.1 × 4.6	40
–	SOT324	3.58	6.4 × 19.0 × 4.5	32

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOD119

DEVICE PART	SUBSTANCE	MASS (mg)
flange	Cu(1)	4120
leadframe	FeNi42(2)	270
brazing alloy	AgCu28	20
encapsulation	Al_2O_3	200
heat spreader	BeO, plated with Mo/Ni/Au	540
active device	doped Si	10
glue	polyamide	40

Notes

1. In some types: WCu15 flange.
2. In SOT119A1 and SOT289: FeNiCo leadframe.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2

Environmental information Chapter 7

STUD-MOUNTED CERAMIC RF POWER TRANSISTORS

REFERENCE	PACKAGE CODE[1]	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT120A	3.00	ϕ 9.8 × 18.8	40
–	SOT122A	1.90	ϕ 7.6 × 17.0	40
–	SOT147	11.40	ϕ 13.0 × 20.9	40
–	SOT172A	1.40	ϕ 5.4 × 16.0	40

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOD122A

DEVICE PART	SUBSTANCE	MASS (mg)
stud	Cu	800
leadframe	FeNi42[1]	150
nut	CuZn37, Ni plated	630
brazing alloy	AgCu28	30
encapsulation	Al_2O_3	120
heat spreader	BeO, plated with Mo/Ni/Au	120
active device	doped Si	10
glue	polyamide	40

Notes

1. SOT122A2: FeNiCo leadframe.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2

Environmental information Chapter 7

CERAMIC RF POWER TRANSISTORS IN PILL PACKAGE

REFERENCE	PACKAGE CODE[(1)]	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOT119D	1.60	ϕ 13.0 × 4.5	40
–	SOT122D	0.70	ϕ 7.6 × 4.1	40
–	SOT172D	0.30	ϕ 5.4 × 3.6	40

Note

1. Ceramic packages without flange or stud (so called “pill”-packages) have a similar composition, quantities may vary.

Chemical content for group representative SOD119D

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	FeNi42[(1)]	370
brazing alloy	AgCu28	30
encapsulation	Al_2O_3	320
heat spreader	BeO, plated with Mo/Ni/Au	850
active device	doped Si	10
glue	polyamide	20

Note

1. FeNiCo in SOT119A1.

PACKING MATERIAL (BLISTER PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	157
foam	polyethylene	27.2
blisters	polystyrene	46
labels	paper	0.8
tape	polypropylene	1
seal	acrylate	0.2

Environmental information Chapter 7

POWER TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE[1]	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-220	SOT78	1.950	10.3 × 9.9 × 4.5	1000
–	SOT82	0.750	11.1 × 7.8 × 2.8	1000
–	SOT93	4.930	15.2 × 12.7 × 4.6	500
–	SOT186	1.950	10.2 × 9.5 × 4.6	1000
–	SOT186A	2.500	10.3 × 9.4 × 4.6	1000
–	SOT199	5.500	15.3 × 21.5 × 5.2	500
pentawatt	SOT263	1.700	10.3 × 9.5 × 4.5	1000
–	SOT399	5.890	16 × 27 × 5.8	500

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOT93

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu	3950
	SnPb30 plated	20
solder pellet	SnAg25Sb10	25
encapsulation	OCN-epoxy polymer (SiO_2 < 72%, Sb < 3%, Br < 1%)	920
active device	doped Si	15

PACKING MATERIAL (TUBE PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	123
tubes	polyvinylchloride	700
turn locks	polyvinylchloride	20
labels	paper	15
tape	polypropylene	0.6
seal	acrylate	0.2

SURFACE-MOUNT POWER TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE[1]	MASS (g)	BODY (mm)	PACKING QUANTITY
D2-PAK	SOT404	1.43	10.3 × 9.5 × 4.5	800
–	SOT426	1.46	10.3 × 9.5 × 4.5	800
–	SOT427	1.49	10.3 × 9.5 × 4.5	800
D-PAK	SOT428	0.33	6.2 × 6.7× 2.4	2500
TO-247	SOT429	5.42	15.5 × 20.5× 5.0	500

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOT404

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu, Ni plated	422
solder pellet	SnAg25Sb10[1]	
encapsulation	OCN-epoxy polymer (SiO_2 < 72%, Sb < 3%, Br < 1%)	120
active device	doped Si	

Note

1. Optional PbSn5 solder pellet.

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	180
reel	polystyrene	325
carrier tape	polystyrene, carbon loaded	200
cover tape	polyester	13.7
labels	paper	2.1
tape	polypropylene	0.6
seal	acrylate	0.2

Environmental information

Chapter 7

MAGNETIC SENSOR PACKAGES

REFERENCE	PACKAGE CODE(1)	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOT453A	230	18.0 × 4.4 × 1.6	1000
–	SOT453B	1600	18.0 × 8.2 × 7.0	750
–	SOT453C	645	18.0 × 4.4 × 4.5	750

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOT453B

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	CuZr0.2 with Ag spot	76
bond-wire	Au	<0.2
solder layer	Sn	7
encapsulation	OCN-epoxy polymer (SiO_2 < 72%, Sb < 3%, Br < 2%)	110
magnet	$BaFe_{12}O_{19}$	1400
magnetic field sensor device	Si with thin metal films	1.2
active device	doped Si, Al, TiW	4.8

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	300
reel	polystyrene	350
carrier tape	polystyrene, carbon loaded	140
cover tape	polyester	24
labels	paper	5
seal	acrylate	1

Environmental information Chapter 7

MEDIUM-POWER TRANSISTORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE[1]	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-126	SOT32	0.694	$11.1 \times 7.8 \times 2.8$	1000
TO-202	SOT128	1.528	$11.1 \times 7.8 \times 2.7$	1000

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOT128

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	Cu, Co + Au plated	863
	SnPb plated	15
active device	doped Si	10
encapsulation	silica filled epoxy plastic (Sb < 3%, Br < 2%)	640

PACKING MATERIAL (TUBE PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	123
tubes	polyvinylchloride	836
end stops	polyvinylchloride	38
labels	paper	15
tape	polypropylene	0.6
seal	acrylate	0.2

Environmental information Chapter 7

SMALL-SIGNAL TRANSISTORS AND SENSORS IN PLASTIC PACKAGE

REFERENCE	PACKAGE CODE	MASS (g)	BODY (mm)	PACKING QUANTITY
–	SOD70	0.2	ϕ 4.4 × 5.0	1000
TO-92	SOT54	0.250	ϕ 4.8 × 5.2	2000
–	SOT195	0.166	5.0 × 4.4 × 1.6	1000

Chemical content for group representative SOT54

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	CuZn15, Co + Au plated	113
	SnPb plated	1.5
active device	doped Si	0.5
encapsulation[1]	OCN-epoxy polymer (SiO_2 < 72%, Sb < 4%, Br < 0.6%)	135

Note

1. Alternative: two-shot encapsulation of epoxy and PPS.

PACKING MATERIAL (AMMO PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	97.5
carrier tape	kraft paper	110
buffer	cardboard	20

Environmental information Chapter 7

TRANSISTORS IN METAL PACKAGE

REFERENCE	PACKAGE CODE(1)	MASS (g)	BODY (mm)	PACKING QUANTITY
TO-39	SOT5	0.97	ϕ 8.5 × 6.6	1000
TO-18	SOT18	0.31	ϕ 4.8 × 5.3	5000

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representative SOT18

DEVICE PART	SUBSTANCE	MASS (mg)
metal envelope + leads	FeNi28Co18	240
wires + solder	Au	2
solder layer	Sn	5
part of encapsulation	glass	62
active device	doped Si	1

PACKING MATERIAL (BULK PACK)

PACKING PART	SUBSTANCE	MASS (g)
box	cardboard	125.4
bag	polyethylene	14.5
label	paper	1.4

Environmental information Chapter 7

TRANSISTORS IN PLASTIC PACKAGE, SMD

REFERENCE	PACKAGE CODE[1]	MASS (mg)	BODY (mm)	PACKING QUANTITY
–	SOT23	8	2.9 × 1.3 × 0.9	3000
–	SOT89	50	4.5 × 2.5 × 1.5	1000
–	SOT143	8	2.9 × 1.3 × 0.9	3000
–	SOT223	124	6.5 × 3.5 × 1.6	1000
SC70-3	SOT323	5	2.0 × 1.3 × 0.9	3000
–	SOT343	6	2.0 × 1.3 × 0.9	3000
SC-59	SOT346	8	2.9 × 1.3 × 1.5	3000
SC70-5	SOT353	5	2.0 × 1.3 × 0.9	3000
SC70-6	SOT363	5	2.0 × 1.3 × 0.9	3000
SC-75	SOT416	2.5	1.6 × 0.8× 0.8	3000
SC-74	SOT457	11	2.9 × 1.0 × 1.5	3000

Note

1. All packages have a similar composition, quantities may vary.

Chemical content for group representiveSOT23

DEVICE PART	SUBSTANCE	MASS (mg)
leadframe	FeNi42[1]	2.6
	SnPb20 plated	0.3
active device	doped Si	0.1
encapsulation	OCN-epoxy polymer (SiO_2 < 72%, Sb < 2%, Br < 1%)	5.0

Note

1. Optional: copper-plated NiFe leadframe.

PACKING MATERIAL (REEL PACK)

PACKING PART	SUBSTANCE	Mass (g)
box	cardboard	56
reel	polystyrene	74
carrier tape	polycarbonate, carbon loaded	22.6
cover tape	polyester	4
labels	paper	2.1
seal	acrylate	0.2

CHAPTER 8

DATA HANDBOOK SYSTEM

Data handbook system Chapter 8

DATA HANDBOOK SYSTEM

Philips Semiconductors data handbooks contain all pertinent data available at the time of publication and each is revised and reissued regularly.

Loose data sheets are sent to subscribers to keep them up-to-date on additions or alterations made during the lifetime of a data handbook.

Catalogues are available for selected product ranges (some catalogues are also on floppy discs).

Our data handbook titles are listed here.

Integrated circuits

Book	*Title*
IC01	Semiconductors for Radio, Audio and CD/DVD Systems
IC02	Semiconductors for Television and Video Systems
IC03	Semiconductors for Wired Telecom Systems
IC04	HE4000B Logic Family CMOS
IC05	Advanced Low-power Schottky (ALS) Logic
IC06	High-speed CMOS Logic Family
IC11	General-purpose/Linear ICs
IC12	I^2C Peripherals
IC13	Programmable Logic Devices (PLD)
IC14	8048-based 8-bit Microcontrollers
IC15	FAST TTL Logic Series
IC16	CMOS ICs for Clocks, Watches and Real Time Clocks
IC17	Semiconductors for Wireless Communications
IC18	Semiconductors for In-Car Electronics
IC19	ICs for Data Communications
IC20	80C51-based 8-bit Microcontrollers
IC22	Multimedia ICs
IC23	BiCMOS Bus Interface Logic
IC24	Low Voltage CMOS & BiCMOS Logic
IC25	16-bit 80C51XA Microcontrollers (eXtended Architecture)
IC26	Integrated Circuit Packages
IC27	Complex Programmable Logic Devices

Discrete semiconductors

Book	*Title*
SC01	Small-signal and Medium-power Diodes
SC03	Power Thyristors and Triacs
SC04	Small-signal Transistors
SC05	Video Transistors and Modules for Monitors
SC06	Power Bipolar Transistors
SC07	Small-signal Field-effect Transistors
SC11	Power Diodes
SC13	PowerMOS Transistors
SC14	RF Wideband Transistors
SC16	Wideband Hybrid Amplifier Modules for CATV
SC17	Semiconductor Sensors
SC18	Discrete Semiconductor Packages
SC19	RF & Microwave Power Transistors, RF Power Modules and Circulators/Isolators

MORE INFORMATION FROM PHILIPS SEMICONDUCTORS?

For more information about Philips Semiconductors data handbooks, catalogues and subscriptions contact your nearest Philips Semiconductors national organization, select from the **address list on the back cover of this handbook.** Product specialists are at your service and enquiries are answered promptly.

Data handbook ststem

Chapter 8

OVERVIEW OF PHILIPS COMPONENTS DATA HANDBOOKS

Our sister product division, Philips Components, also has a comprehensive data handbook system to support their products. Their data handbook titles are listed here.

Display Components

Book	*Title*
DC01	Colour Television and Multimedia Tubes
DC02	Monochrome Monitor Tubes and Deflection Units
DC03	Television Tuners, Coaxial Aerial Input Assemblies
DC04	Colour Monitor and Multimedia Tubes
DC05	Wire Wound Components

Advanced Ceramics & Modules

ACM1 (MA01)	Soft Ferrites
ACM2	Discrete Ceramics
ACM3 (MA03)	Piezoelectric Ceramics and Speciality Ferrites

BC Components

PA01	Electrolytic Capacitors
PA02	Varistors, Thermistors and Sensors
PA03	Potentiometers
PA04	Variable Capacitors
PA05	Film Capacitors
PA06	Ceramic Capacitors
PA06a	Surface Mounted Ceramic Multilayer Capacitors
PA06b	Leaded Ceramic Capacitors
PA08	Fixed Resistors
PA10	Quartz Crystals
PA11	Quartz Oscillators

MORE INFORMATION FROM PHILIPS COMPONENTS?

For more information contact your nearest Philips Components national organization shown in the following list.

Australia: North Ryde, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466
Austria: Wien, Tel. +43 1 60 101 12 41, Fax. +43 1 60 101 12 11
Belarus: Minsk, Tel. +375 172 200 924/733, Fax. +375 172 200 773
Benelux: Eindhoven, Tel. +31 40 2783 749, Fax. +31 40 2788 399
Brazil: São Paolo, Tel. +55 11 821 2333, Fax. +55 11 829 1849
Canada: Scarborough, Tel. 1 416 292 5161, Fax. 1 416 754 6248
China: Shanghai, Tel. +86 21 6354 1088, Fax. +86 21 6354 1060
Denmark: Copenhagen, Tel. +45 32 883 333, Fax. +45 31 571 949
Finland: Espoo, Tel. 358 9 615 800, Fax. 358 9 615 80510
France: Suresnes, Tel. +33 1 4099 6161, Fax. +33 1 4099 6493
Germany: Hamburg, Tel. +49 40 2489-0, Fax. +49 40 2489 1400
Greece: Tavros, Tel. +30 1 4894 339/+30 1 4894 239, Fax. +30 1 4814 240
Hong Kong: Kowloon, Tel. +852 2784 3000, Fax. +852 2784 3003
India: Mumbai, Tel. +91 22 4930 311, Fax. +91 22 4930 966/4950 304
Indonesia: Jakarta, Tel. +62 21 794 0040, Fax. +62 21 794 0080
Ireland: Dublin, Tel. +353 1 7640 203, Fax. +353 1 7640 210
Israel: Tel Aviv. Tel. +972 3 6450 444, Fax. +972 3 6491 007
Italy: Milano, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557
Japan: Tokyo, Tel. +81 3 3740 5135, Fax. +81 3 3740 5035
Korea (Republic of): Seoul, Tel. +82 2 709 1472, Fax. +82 2 709 1480
Malaysia: Pulau Pinang, Tel. +60 3 750 5213, Fax. +60 3 757 4880
Mexico: El Paso, Tel. +52 915 772 4020, Fax. +52 915 772 4332
New Zealand: Auckland, Tel. +64 9 815 4000, Fax. +64 9 849 7811
Norway: Oslo, Tel. +47 22 74 8000, Fax. +47 22 74 8341
Pakistan: Karachi, Tel. +92 21 587 4641-49, Fax. +92 21 577 035/+92 21 587 4546
Philippines: Manila, Tel. +63 2 816 6345, Fax. +63 2 817 3474
Poland: Warszawa, Tel. +48 22 612 2594, Fax. +48 22 612 2327
Portugal: Linda-A-Velha, Tel. +351 1 416 3160/416 3333, Fax. +351 1 416 3174/416 3366
Russia: Moscow, Tel. +7 95 755 6918, Fax. +7 95 755 6919
Singapore: Singapore, Tel. +65 350 2000, Fax. +65 355 1758
South Africa: Johannesburg, Tel. +27 11 470 5911, Fax. +27 11 470 5494
Spain: Barcelona, Tel. +34 93 301 63 12, Fax. +34 93 301 42 43
Sweden: Stockholm, Tel. +46 8 5985 2000, Fax. +46 8 5985 2745
Switzerland: Zürich, Tel. +41 1 488 22 11, Fax. +41 1 481 7730
Taiwan: Taipei, Tel. +886 2 2134 2900, Fax. +886 2 2134 2929
Turkey: Istanbul, Tel. +90 212 279 2770, Fax. +90 212 282 6707
United Kingdom: Dorking, Tel. +44 1306 512 000, Fax. +44 1306 512 345
United States:

- San Jose, Tel. +1 408 570 5600, Fax. +1 408 570 5700
- Ann Arbor, Tel. +1 734 996 9400, Fax. +1 734 761 27760

Yugoslavia (Federal Republic of): Belgrade, Tel. +381 11 625 344 / +381 11 3341 299, Fax. +381 11 635 777

Internet:

- Advanced Ceramics & Modules: www.acm.components.philips.com
- Display Components: www.dc.comp.philips.com

For all other countries apply to:
Philips Components, Marketing Communications, Building BF-1, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31-40-2722722

North American Sales Offices, Representatives and Distributors

PHILIPS SEMICONDUCTORS
811 East Arques Avenue
P.O. Box 3409
Sunnyvale, CA 94088-3409

ALABAMA
Huntsville
Philips Semiconductors
Phone: (256) 464-9101
(256) 464-0111

Elcom, Inc.
Phone: (256) 830-4001

ARIZONA
Scottsdale
Thom Luke Sales, Inc.
Phone: (602) 451-5400

Tempe
Philips Semiconductors
Phone: (602) 820-2225

CALIFORNIA
Calabasas
Philips Semiconductors
Phone: (818) 880-6304

Centaur Corporation
Phone: (818) 878-5800

Granite Bay
B.A.E. Sales, Inc.
Phone: (916) 652-6777

Irvine
Philips Semiconductors
Phone: (949) 453-0770

Centaur Corporation
Phone: (949) 261-2123

San Diego
Philips Semiconductors
Phone: (619) 560-0242

Centaur Corporation
Phone: (619) 278-4950

San Jose
B.A.E. Sales, Inc.
Phone: (408) 452-8133

Sunnyvale
Philips Semiconductors
Phone: (408) 991-3737

COLORADO
Englewood
Philips Semiconductors
Phone: (303) 792-9011

Thom Luke Sales, Inc.
Phone: (303) 649-9717

CONNECTICUT
Wallingford
JEBCO, Inc.
Phone: (203) 265-1318

FLORIDA
(Norcross, Georgia)
Elcom, Inc.
Phone: (770) 447-8200

GEORGIA
Norcross
Elcom, Inc.
Phone: (770) 447-8200

IDAHO
(Englewood, Colorado)
Thom Luke Sales, Inc.
Phone: (303) 649-9717

ILLINOIS
Itasca
Philips Semiconductors
Phone: (630) 250-0050

INDIANA
Kokomo
Philips Semiconductors
Phone: (765) 459-5355

Leo
Mohrfield Marketing, Inc.
Phone: (219) 627-5355

KANSAS
(Bloomington, Minnesota)
High Technology Sales, Inc.
Phone: (612) 844-9933

KENTUCKY
(Indianapolis, Indiana)
Mohrfield Marketing, Inc.
Phone: (317) 546-6969

MARYLAND
(Rockville Centre, New York)
S-J Associates, Inc.
Phone: (516) 536-4242

MASSACHUSETTS
Westford
Philips Semiconductors
Phone: (978) 692-6211

MICHIGAN
Farmington Hills
Philips Semiconductors
Phone: (248) 848-7600

Novi
Mohrfield Marketing, Inc.
Phone: (248) 380-8100

MINNESOTA
Bloomington
High Technology Sales, Inc.
Phone: (612) 844-9933

MISSOURI
(Bloomington, Minnesota)
High Technology Sales, Inc.
Phone: (612) 844-9933

NEBRASKA
(Bloomington, Minnesota)
High Technology Sales, Inc.
Phone: (612) 844-9933

NEW JERSEY
Toms River
Philips Semiconductors
Phone: (732) 505-1200
(732) 240-1479

NEW MEXICO
(Scottsdale, Arizona)
Thom Luke Sales, Inc.
Phone: (602) 451-5400

NEW YORK
Liverpool
JEBCO, Inc.
Phone: (315) 451-0800

Rockville Centre
S-J Associates, Inc.
Phone: (516) 536-4242

NORTH CAROLINA
Cary
Philips Semiconductors
Phone: (919) 462-1332
(919) 462-6361

Raleigh
Elcom, Inc.
Phone: (919) 743-5200

OHIO
Columbus
Mohrfield Marketing, Inc.
Phone: (614) 481-5451

Dayton
Mohrfield Marketing, Inc.
Phone: (937) 298-7322

Solon
Mohrfield Marketing, Inc.
Phone: (440) 349-2700

OKLAHOMA
(Richardson, Texas)
OM Associates, Inc.
Phone: (972) 690-6746

OREGON
Beaverton
Cascade-Tech
Phone: (503) 645-9660

PENNSYLVANIA
Ambrioge
Mohrfield Marketing, Inc.
Phone: (724) 251-0576

(Mt. Laurel, New Jersey)
S-J Associates, Inc.
Phone: (609) 866-1234

TENNESSEE
Dandridge
Philips Semiconductors
Phone: (423) 397-5557

TEXAS
Austin
OM Associates, Inc.
Phone: (512) 794-9971

El Paso
OM Associates, Inc.
Phone: (915) 591-9123

Houston
Philips Semiconductors
Phone: (281) 999-1316

OM Associates, Inc.
Phone: (281) 376-6400

Richardson
Philips Semiconductors
Phone: (972) 644-1610

OM Associates, Inc.
Phone: (972) 690-6746

VIRGINIA
Falls Church
S-J Associates, Inc.
Phone: (703) 533-2233

WASHINGTON
Kirkland
Cascade-Tech
Phone: (425) 822-7299

WISCONSIN
Browndeer
High Technology Sales, Inc.
Phone: (414) 354-9029

CANADA
PHILIPS SEMICONDUCTORS CANADA, LTD.
Calgary, Alberta
Tech-Trek, Ltd.
Phone: (403) 291-6866

Kanata, Ontario
Tech-Trek, Ltd.
Phone: (613) 599-8787

Mississauga, Ontario
Tech-Trek, Ltd.
Phone: (905) 238-0366

Richmond, B.C.
Tech-Trek, Ltd.
Phone: (604) 276-8735

Ville St. Laurent, Quebec
Tech-Trek, Ltd.
Phone: (514) 337-7540

MEXICO
Guadalajara
OM Associates de Mexico, SA de CV
Phone: +52-3-647-7881

El Paso, TX
OM Associates, Inc.
Phone: +1 (915) 591-9123

PUERTO RICO
(Norcross, Georgia)
Elcom, Inc.
Phone: (770) 447-8200

DISTRIBUTORS
Contact one of our local distributors:
Allied Electronics
Arrow Electronics, Inc.
Avnet EMG
Future Electronics
Marshall Industries

03/01/99

Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101 1248,
Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 20 0733, Fax. +375 172 20 0773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 68 9211, Fax. +359 2 68 9102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Sydhavnsgade 23, 1780 COPENHAGEN V,
Tel. +45 33 29 3333, Fax. +45 33 29 3905

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615 800, Fax. +358 9 6158 0920

France: 51 Rue Carnot, BP317, 92156 SURESNES Cedex,
Tel. +33 1 4099 6161, Fax. +33 1 4099 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 2353 60, Fax. +49 40 2353 6300

Hungary: see Austria

India: Philips INDIA Ltd, Band Box Building, 2nd floor,
254-D, Dr. Annie Besant Road, Worli, MUMBAI 400 025,
Tel. +91 22 493 8541, Fax. +91 22 493 0966

Indonesia: PT Philips Development Corporation, Semiconductors Division,
Gedung Philips, Jl. Buncit Raya Kav.99-100, JAKARTA 12510,
Tel. +62 21 794 0040 ext. 2501, Fax. +62 21 794 0080

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, PO Box 18053,
TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Pakistan: see Singapore

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA,
Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 319762,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Al. Vicente Pinzon, 173, 6th floor, 04547-130 SÃO PAULO, SP,
Brazil, Tel. +55 11 821 2333, Fax. +55 11 821 2382

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 93 301 6312, Fax. +34 93 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 5985 2000, Fax. +46 8 5985 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2741 Fax. +41 1 488 3263

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI,
Taiwan Tel. +886 2 2134 2886, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381, Fax. +1 800 943 0087

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 62 5344, Fax.+381 11 63 5777

For all other countries apply to: Philips Semiconductors, International Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

Printed in USA   195001/15.4M/02/pp304   Date of release: April 1999   Document order number: 9397 750 05011

Philips Semiconductors

PHILIPS

Let's make things better.